

LTspice Model

BRT (Bias Resistor Transistor)

ROHM Semiconductor

DTC123JKAT146

Model Information

Model A macro model based on Gummel-Poon model
Call Name MDC_DTC123JKAT146_LT
Pin Assign 1:E 2:B 3:C
File List Model Library MDC_DTC123JKAT146_LT01.lib
 Model Report MDC_DTC123JKAT146_LT.pdf (this file)
Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 20150311 - Rev.002
- Product name DTC123JKAT146
- Company name ROHM Co., Ltd.
- Characteristics ICVCEIB,ICVBETEMP,ICVBETEMP02, HFEICTEMP,VCESATICTEMP

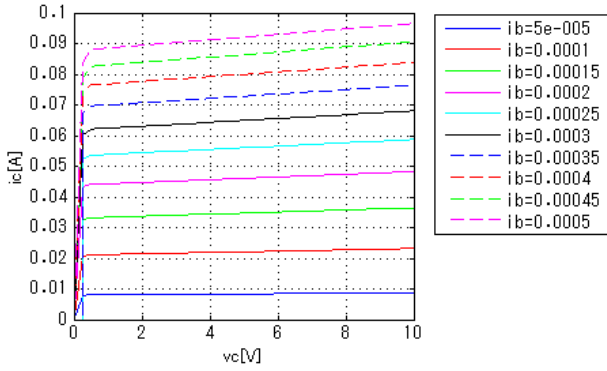
Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

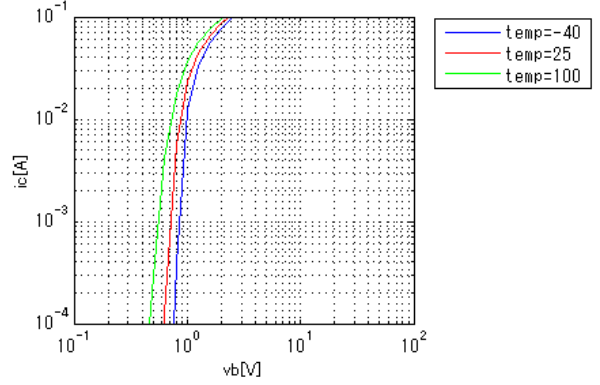
Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
Base current (DC)	0	to	0.1	A
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

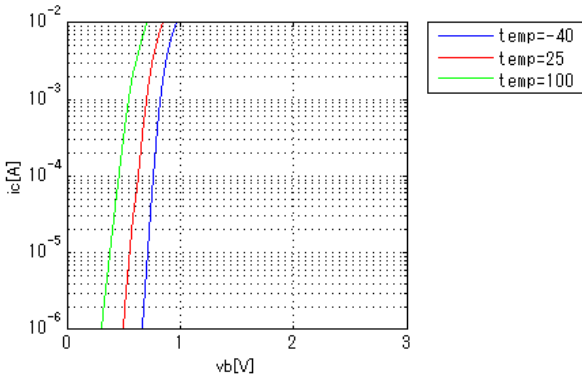
ICVCEIB



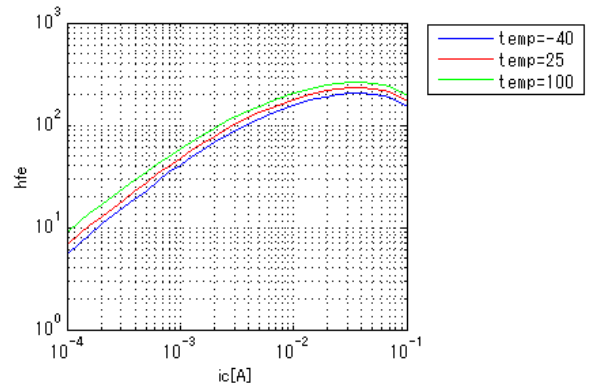
ICVBETEMP



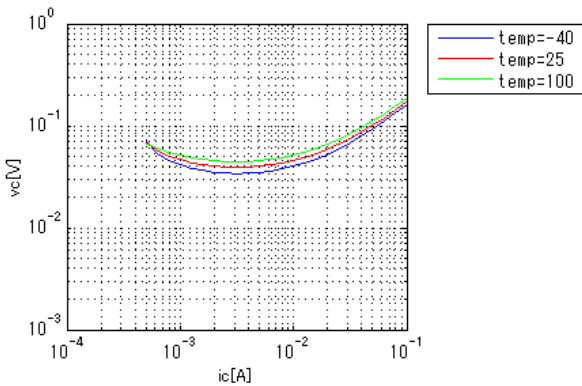
ICVBETEMP02



HFEICTEMP



VCESATICTEMP



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