LTspice Model
PWM Controller
STMicroelectronics
VIPER12A-E

Model Information

Model   A macro model
Call Name MDC_VIPER12A-E_LT
Pin Assign 1:SOURCE 2:SOURCE 3:FB 4:VDD 5:DRAIN 6:DRAIN 7:DRAIN 8:DRAIN
File List   Model Library   MDC_VIPER12A-E_LT.lib
                  Model Report   MDC_VIPER12A-E_LT.pdf (this file)

Verified Simulator Version   LTspice XVII
Note
          Please set Trtol option from 1 to 7 for LTspice Troubles.
          Tool → Control Panel → SPICE → Trtol

References
The information which was used for modeling is as follow:

     [Data Sheet]
          ●Date/Version   Doc ID 11977 Rev 2(3-Dec-2010)
          ●Product name   VIPER12A-E
          ●Company name   STMicroelectronics
     [Application Note]
          ●Date/Version   November 2005
          ●Document name   AN2173
          ●Company name   STMicroelectronics
          ●Date/Version   May 2008
          ●Document name   AN2747
          ●Company name   STMicroelectronics
     [Characteristics listed]
          ●Characteristics   Overvoltage Sequence
                                    Restart duty-cycle
                                    Overvoltage Sequence
                                    Nonisolated buck Converter

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

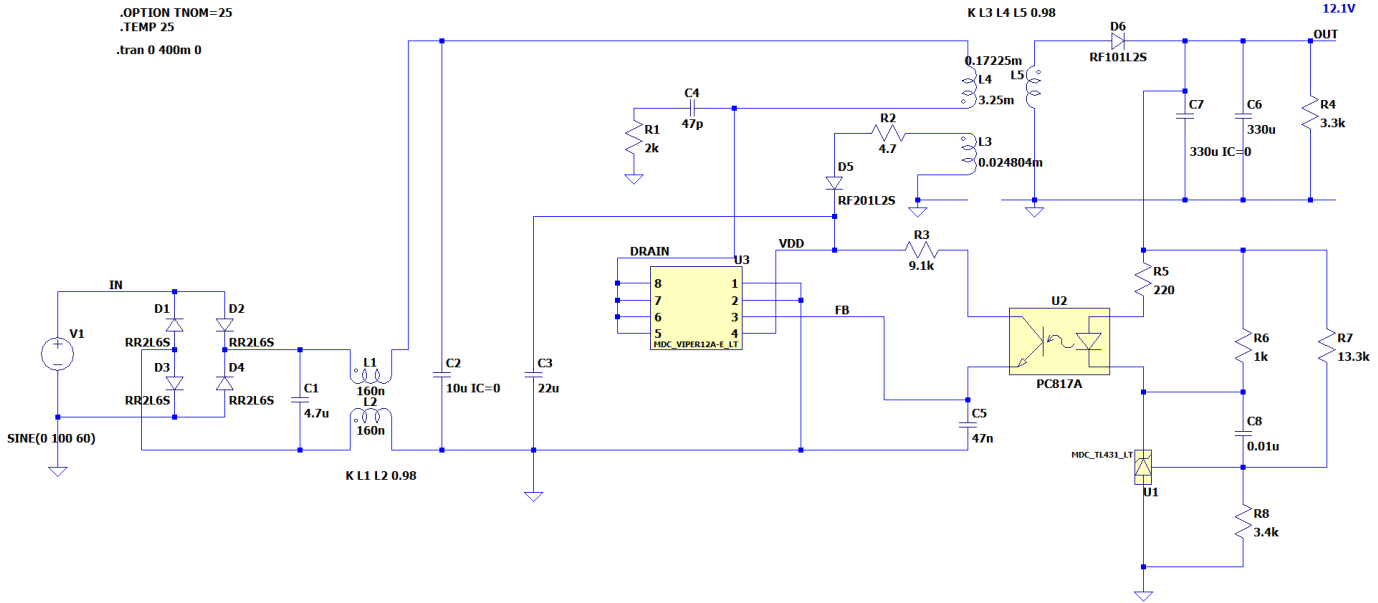| Item	Condition	Unit
Temperature	25	deg C

Model Functions Table

Functions	Implemented
Fixed 60 kHz switching frequency	○
High voltage start-up current source	○
Overvoltage protection	○
9 V to 38 V wide range VDD voltage	○

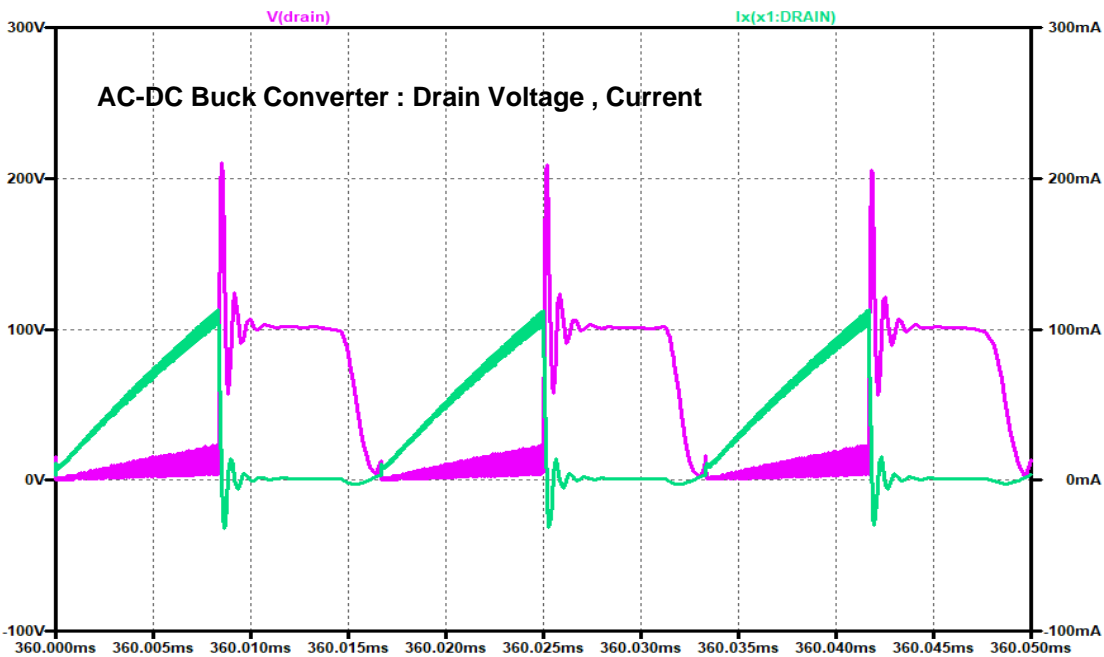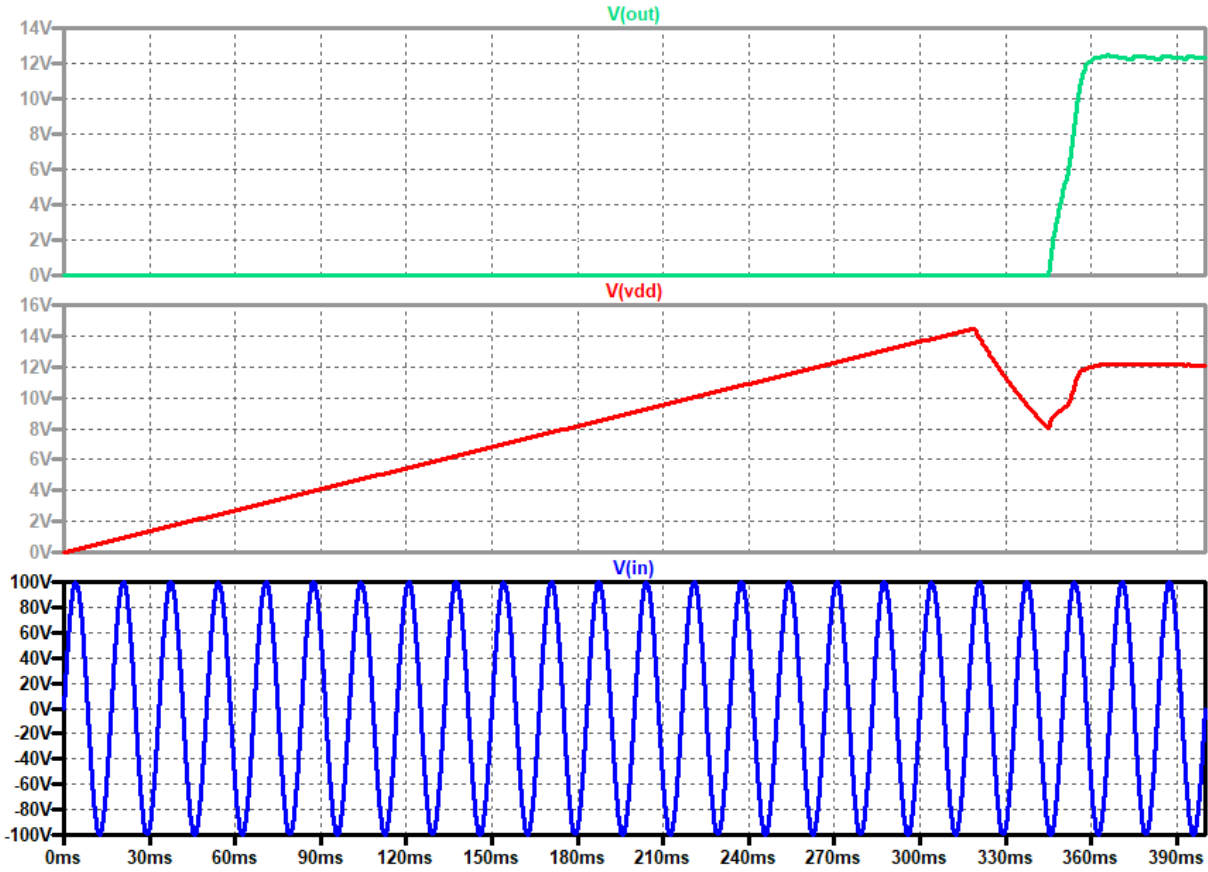Simulation results are following.
Explanatory notes　　— : simulated

AC-DC Buck Converter Testbench

Referred to AN2173
APPLICATION NOTE

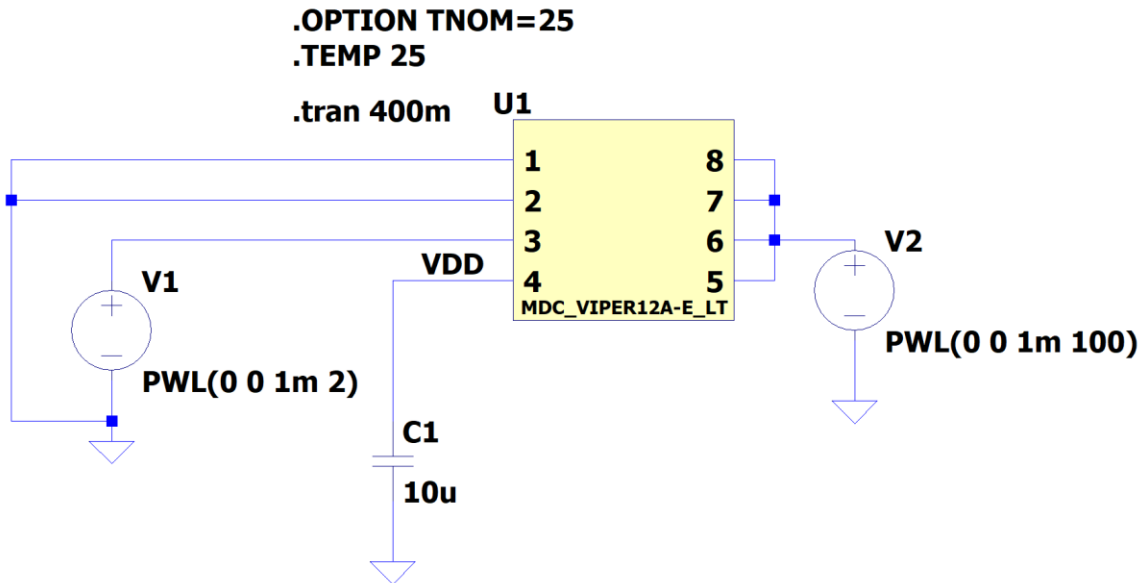Simulation results are following.
Explanatory notes   — : simulated

AC-DC Buck Converter

AC-DC Buck Converter : Drain Voltage , Current

Simulation results are following.
Explanatory notes 　 — : simulated

Restart duty-cycle Testbench

Referred to Data Sheet

.OPTION TNOM=25
.TEMP 25

.tran 400m　U1

```
        ┌──────────────┐
        │ 1          8 │
        │ 2          7 │
        │ 3          6 │  V2
   VDD  │ 4          5 │
        │ MDC_VIPER12A-E_LT │
        └──────────────┘
```

V1

PWL(0 0 1m 2)

C1

10u

PWL(0 0 1m 100)

Simulation results are following.
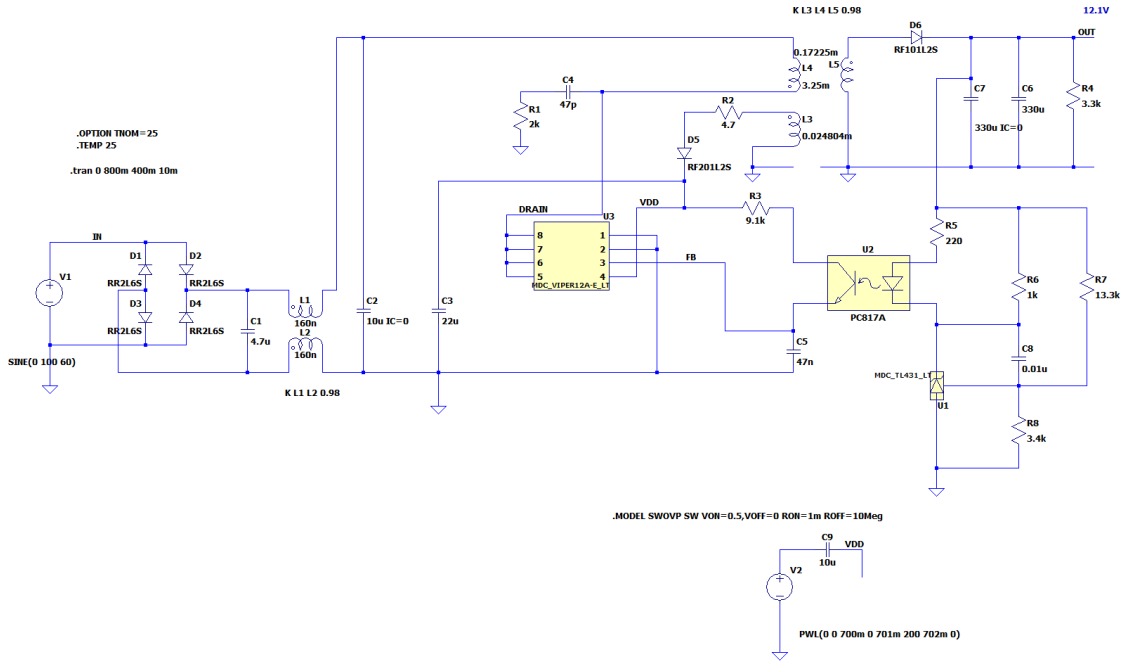Explanatory notes   — : simulated

Restart duty-cycle

Simulation results are following.
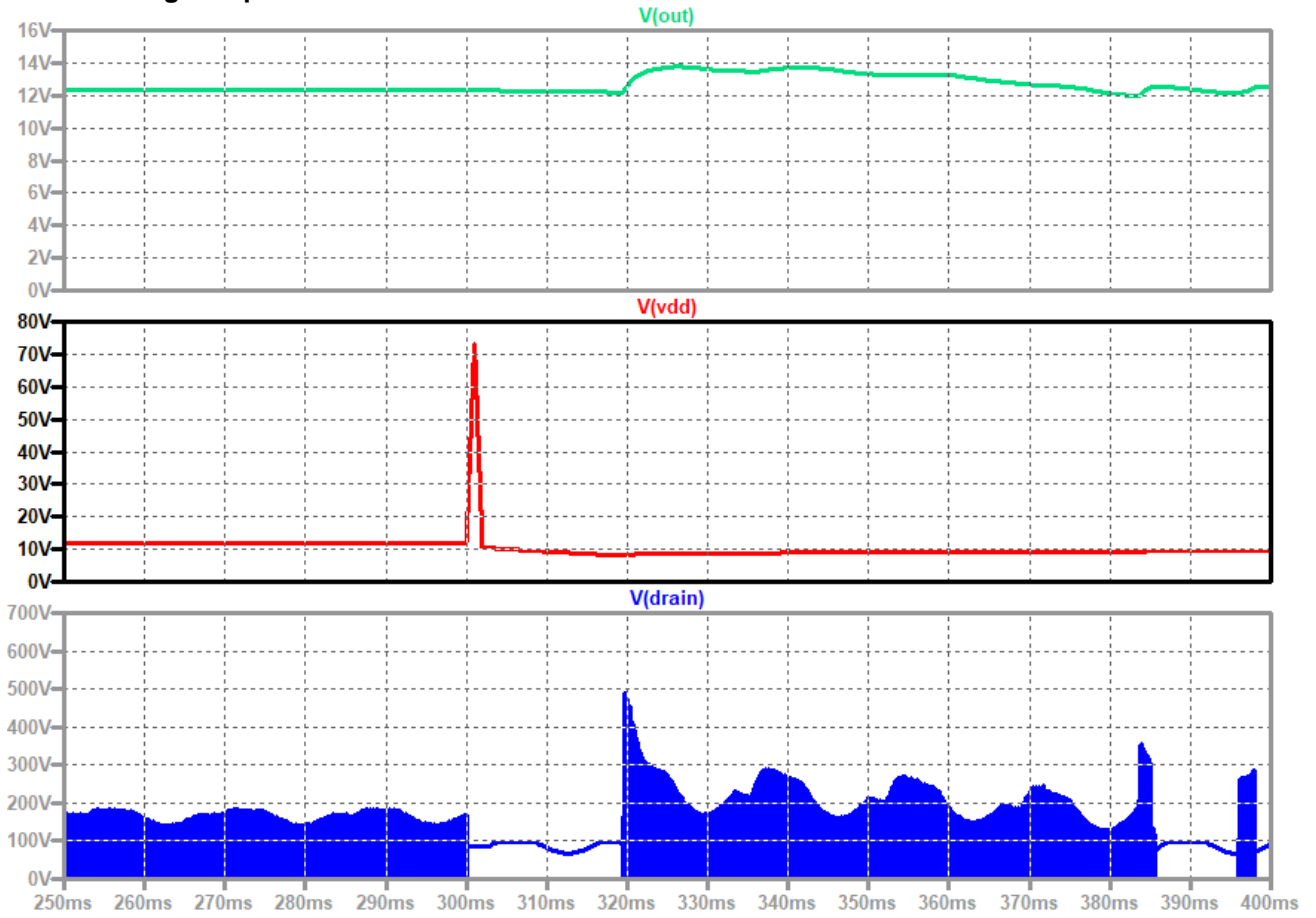Explanatory notes 　 ー : simulated

Overvoltage Sequence Testbench

Referred to AN2173
APPLICATION NOTE
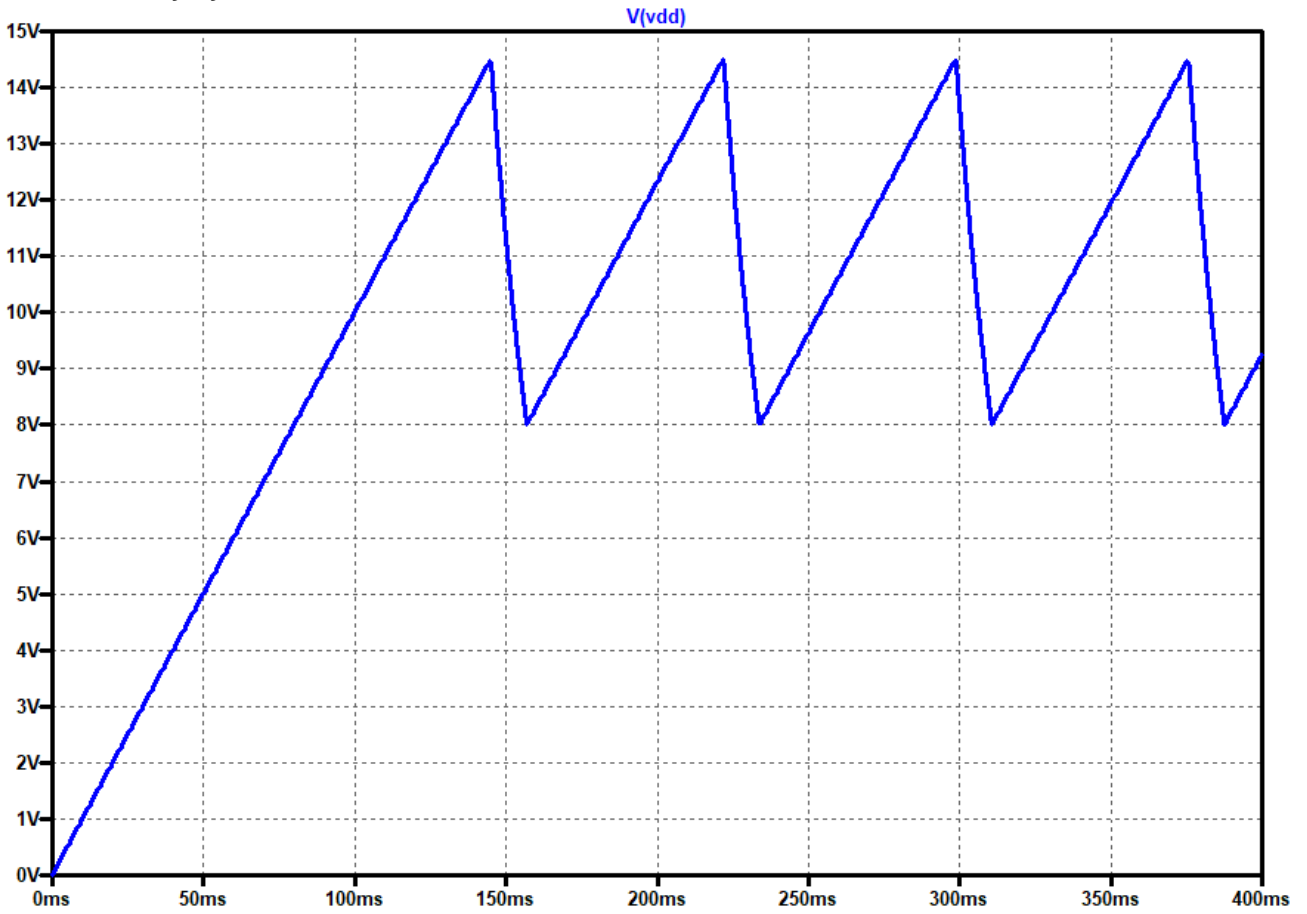
Simulation results are following.
Explanatory notes　　— : simulated
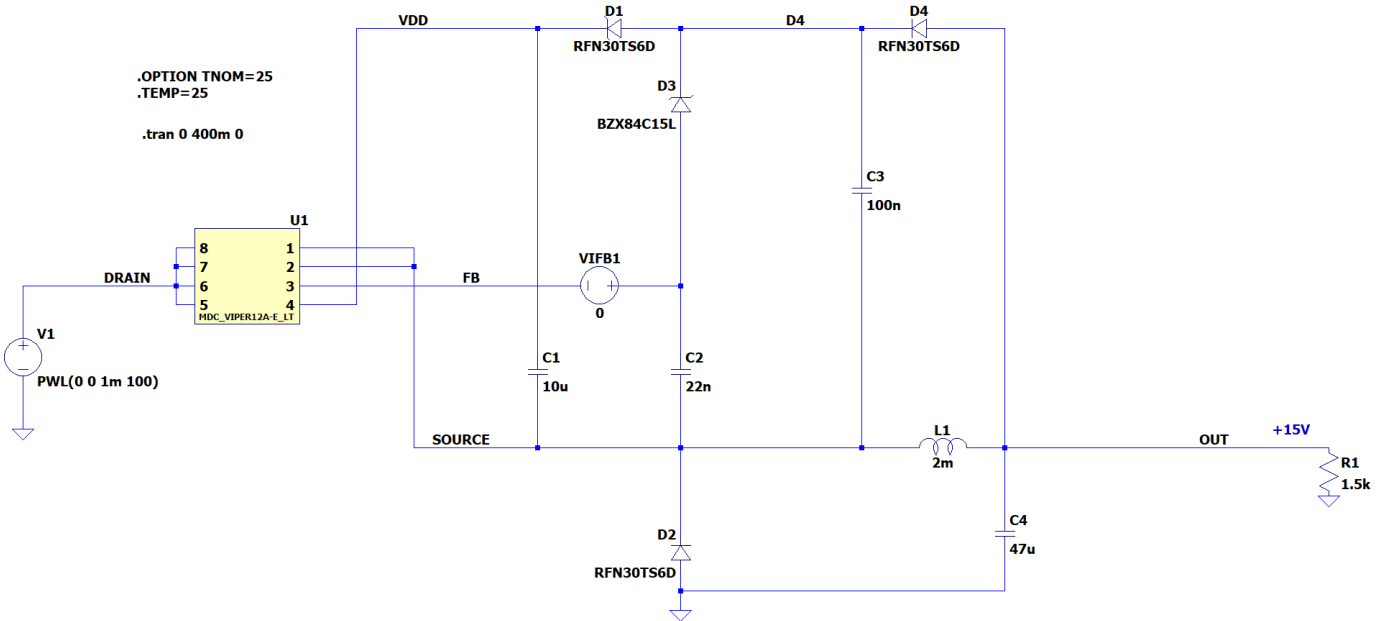
Overvoltage Sequence

Simulation results are following.
Explanatory notes 　－ : simulated
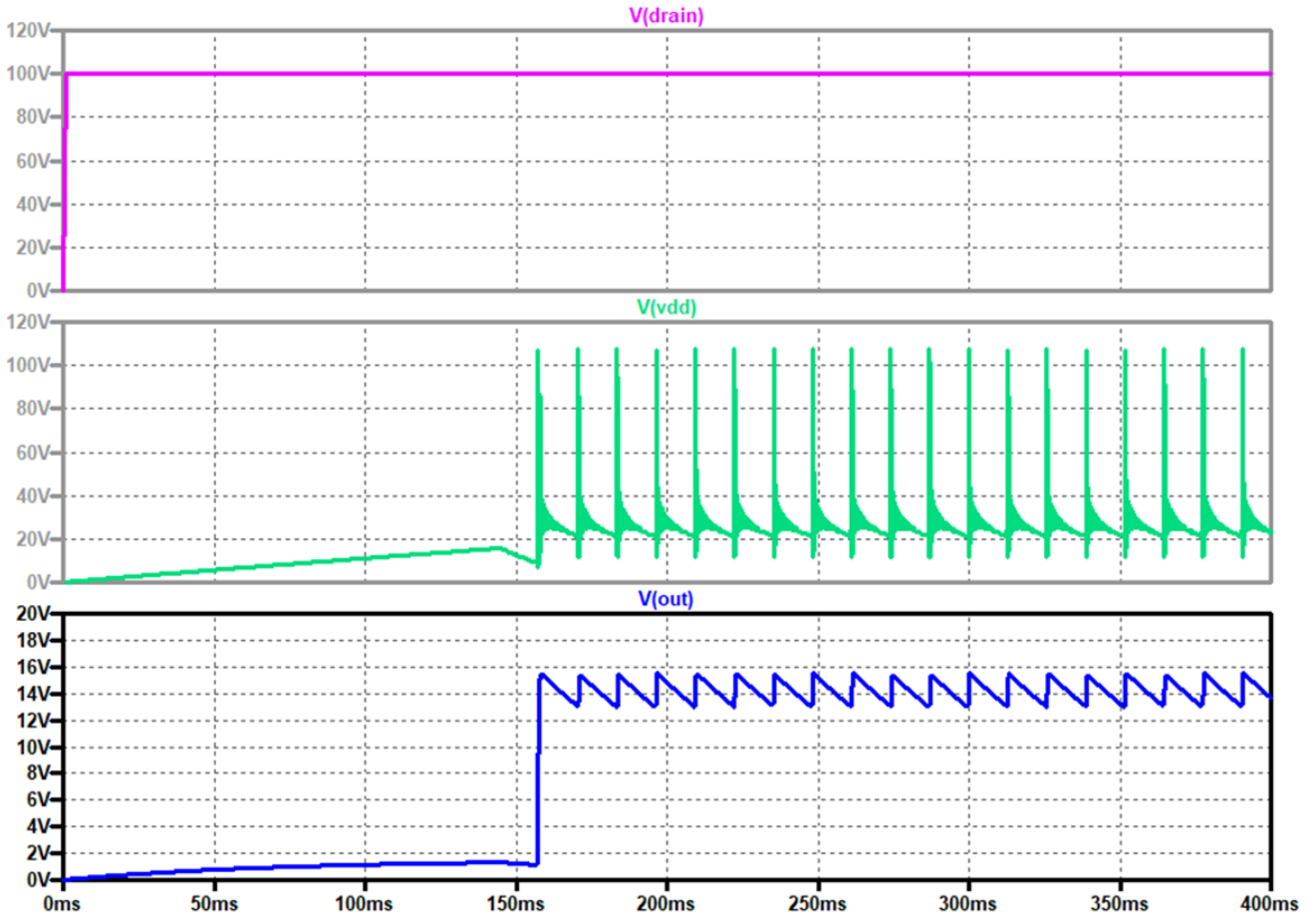
Nonisolated buck Converter Testbench

Referred to AN2747
APPLICATION NOTE

Simulation results are following.
Explanatory notes 　－：simulated

Nonisolated buck Converter

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