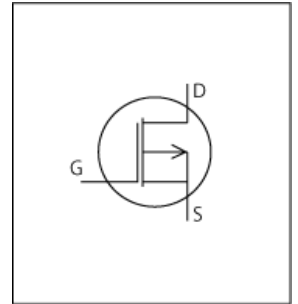


LTspice Model

PMOS

ON

SFT1342-TL-W



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_SFT1342-TL-W_LT
Pin Assign 1:G 2:D 3:S 4:D
File List Model Library MDC_SFT1342-TL-W_LT01.lib
 Model Report MDC_SFT1342-TL-W_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev.2
- Product name SFT1342-TL-W
- Company name ON Semiconductor.
- Characteristics IdVds[Vgs], IdVgs[Temp], Rds(on)Vgs[Id], Rds(on)Temp[Vgs], I
 sVsd[Temp], Crss, Coss, Ciss, VgsQg[Vdd], tdon, tdoff, tf, tr

Simulation Range

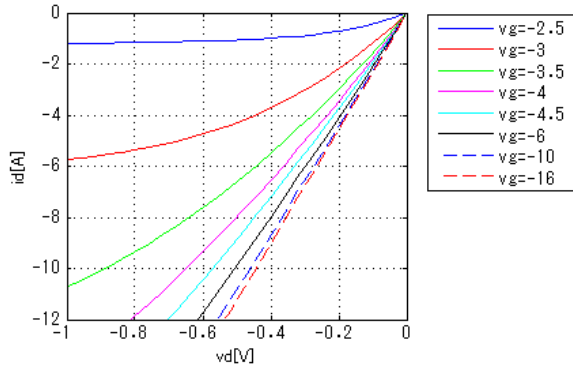
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-60	V
Gate-source voltage (DC)	0	to	-20	V
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

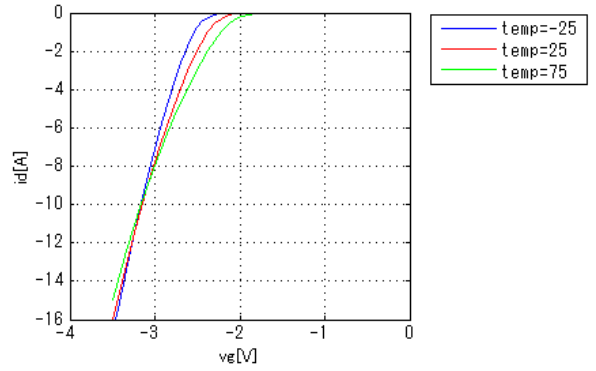
IdVds[Vgs]

Temp. = 25deg C

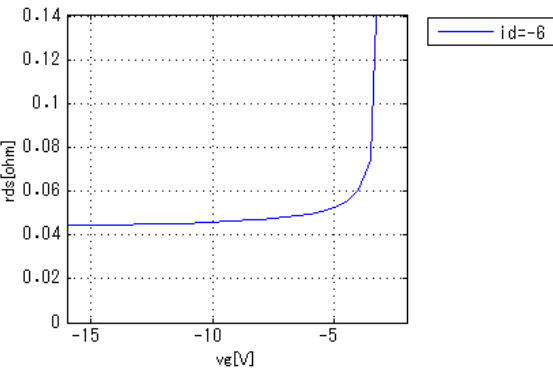


IdVgs[Temp]

Vds = -10V

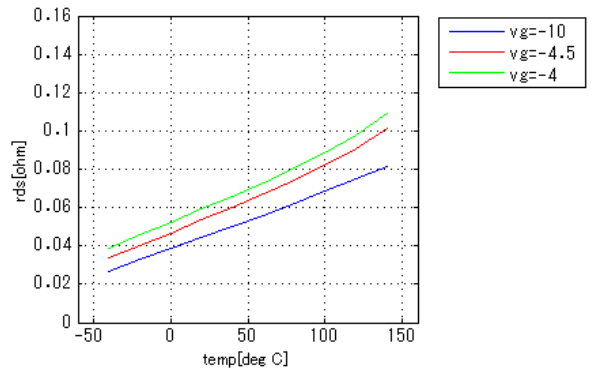


Rds(on)Vgs[Id]

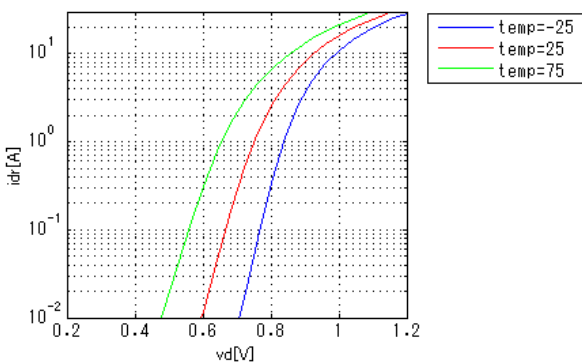


Rds(on)Temp[Vgs]

Id = -6A

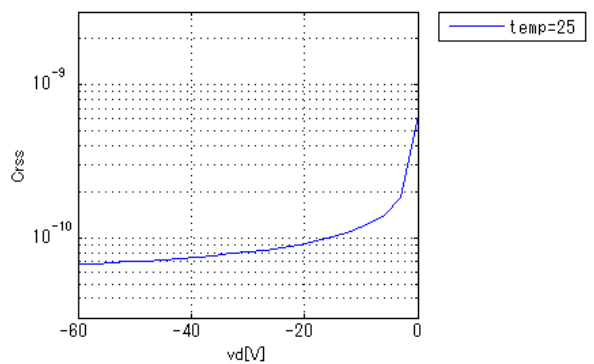


IsVsd[Temp]



Crss

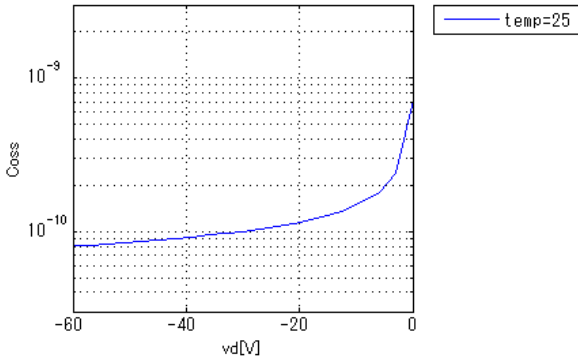
Freq. = 1MHz



Simulation results are following.
 Explanatory notes — : simulated

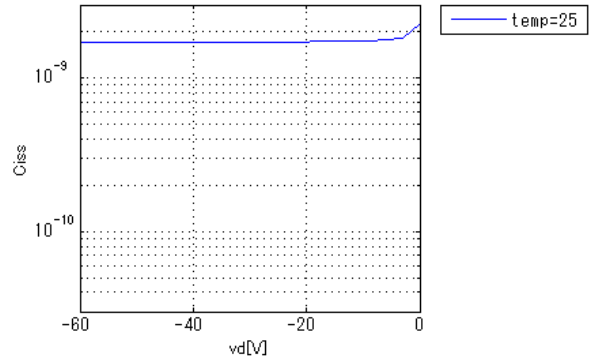
Coss

Freq. = 1MHz



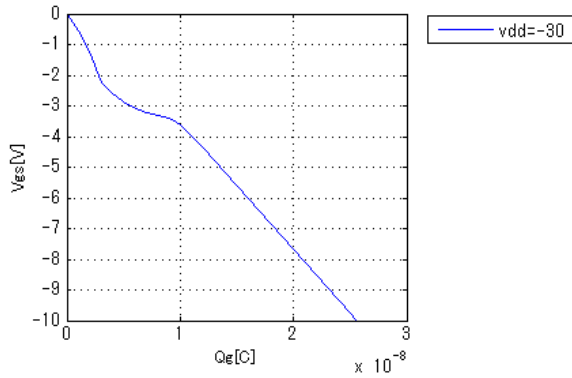
Ciss

Freq. = 1MHz



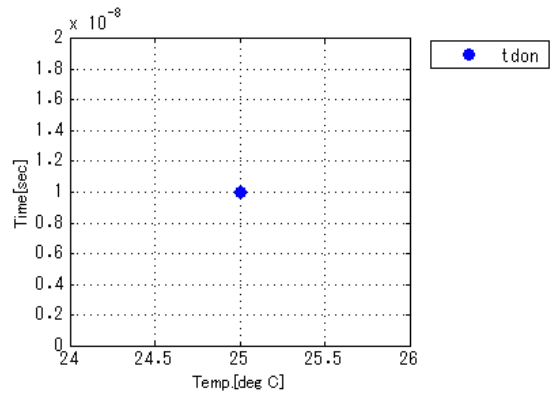
VgsQg[Vdd]

Id = -12A



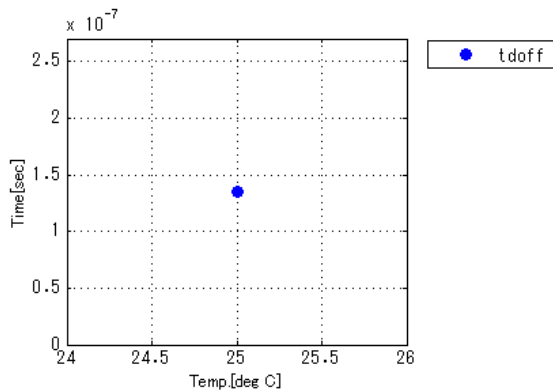
tdon

Vdd = -30V, Id = -6A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



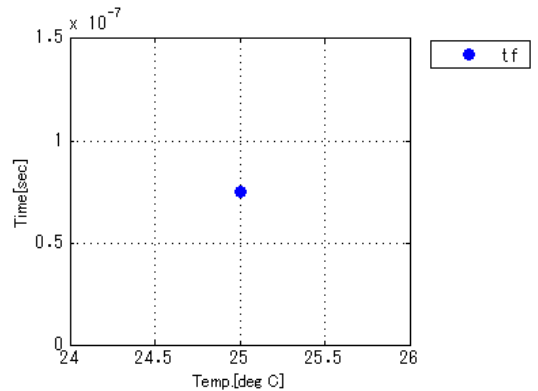
tdoff

Vdd = -30V, Id = -6A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



tf

Vdd = -30V, Id = -6A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm

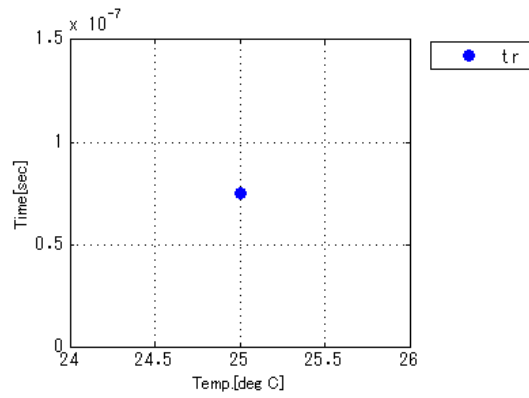


Simulation results are following.

Explanatory notes — : simulated

tr

Vdd = -30V, Id = -6A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



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