PSpice Model
High Stability Isolated Error Amplifier
Analog Devices, Inc.
ADuM3190SRQZ-RL7

Model Information

Model	A macro model
Call Name	MDC_ADuM3190SRQZ-RL7_PS
Pin Assign	1:VDD1 2:GND1 3:VREG1 4:REFOUT1 5:NC 6:EAOUT2 7:EAOUT 8:GND1 9:GND2 10:COMP 11:-IN 12:+IN 13:REFOUT 14:VREG2 15:GND2 16:VDD2
File List	Model Library MDC_ADuM3190SRQZ-RL7_PS01.lib Model Report MDC_ADuM3190SRQZ-RL7_PS.pdf(this file)

Verified Simulator Version PSpice 17.2

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version Rev. A
- ●Product name ADuM3190
- ●Company name Analog Devices, Inc.

[Characteristics listed]

- ●Characteristics Offset Error, Open-Loop Gain, Gain Bandwidth Product, Input, Capacitance, Output Voltage Range, Input Bias Current, Reference Output Voltage, UVLO Positive/Negative Going Threshold, Output Gain, Output -3dB Bandwidth, Output Voltage, EAout/EAout2

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition			Unit
	Min	Typ	Max	
Power Supply Voltage	3.0		20.0	V
Temperature		25.0		deg C

OpAmp

○ : Implemented
× : Not Implemented
— : Not applicable

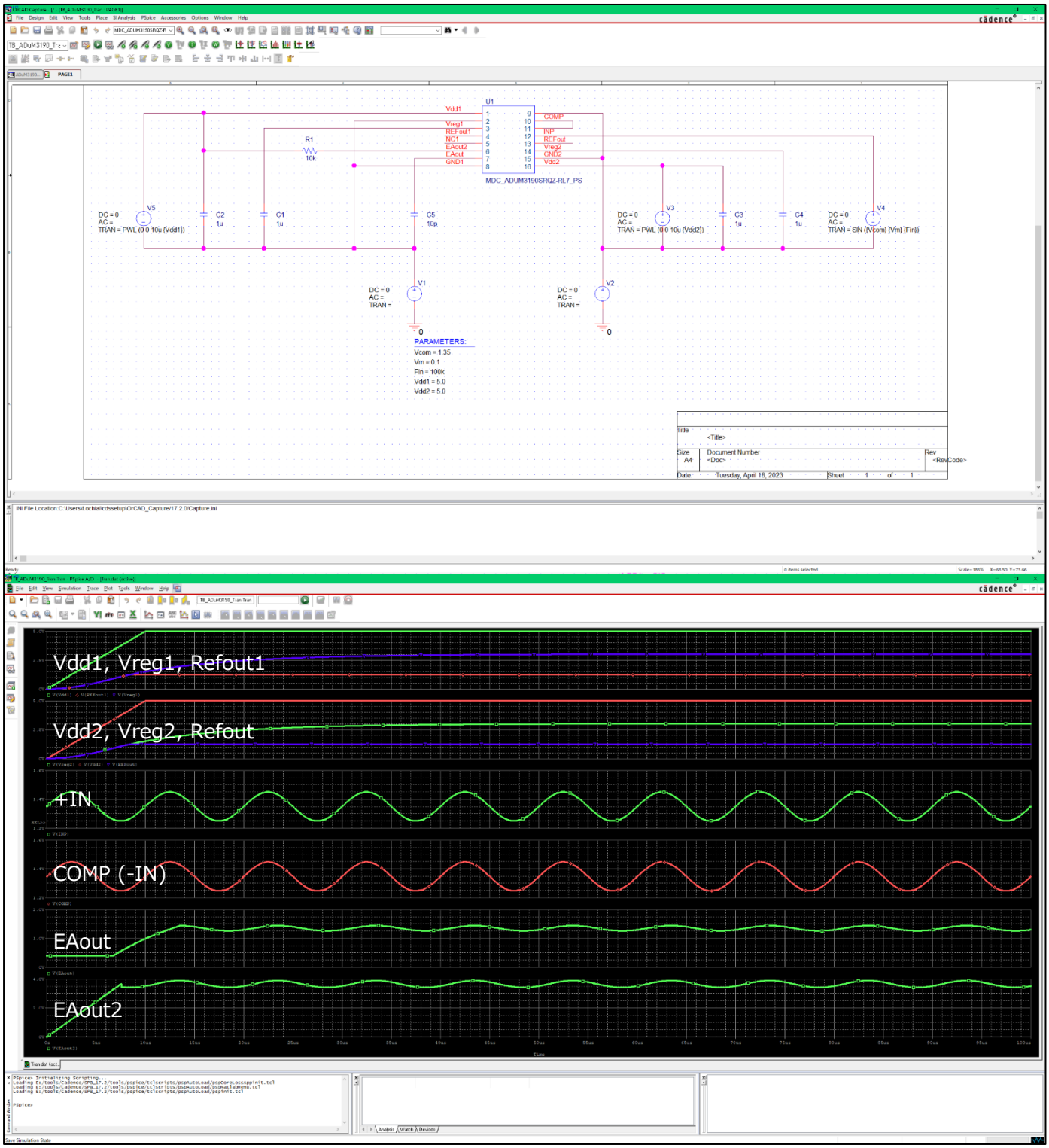
Model Functions Table

RANK=1

Functions	RANK	Implemented
Open Loop Gain	1	○
Unity Frequency	1	○
Input Offset Voltage	1	○
Bias Current	1	○
Maximum output amplitude voltage	1	○

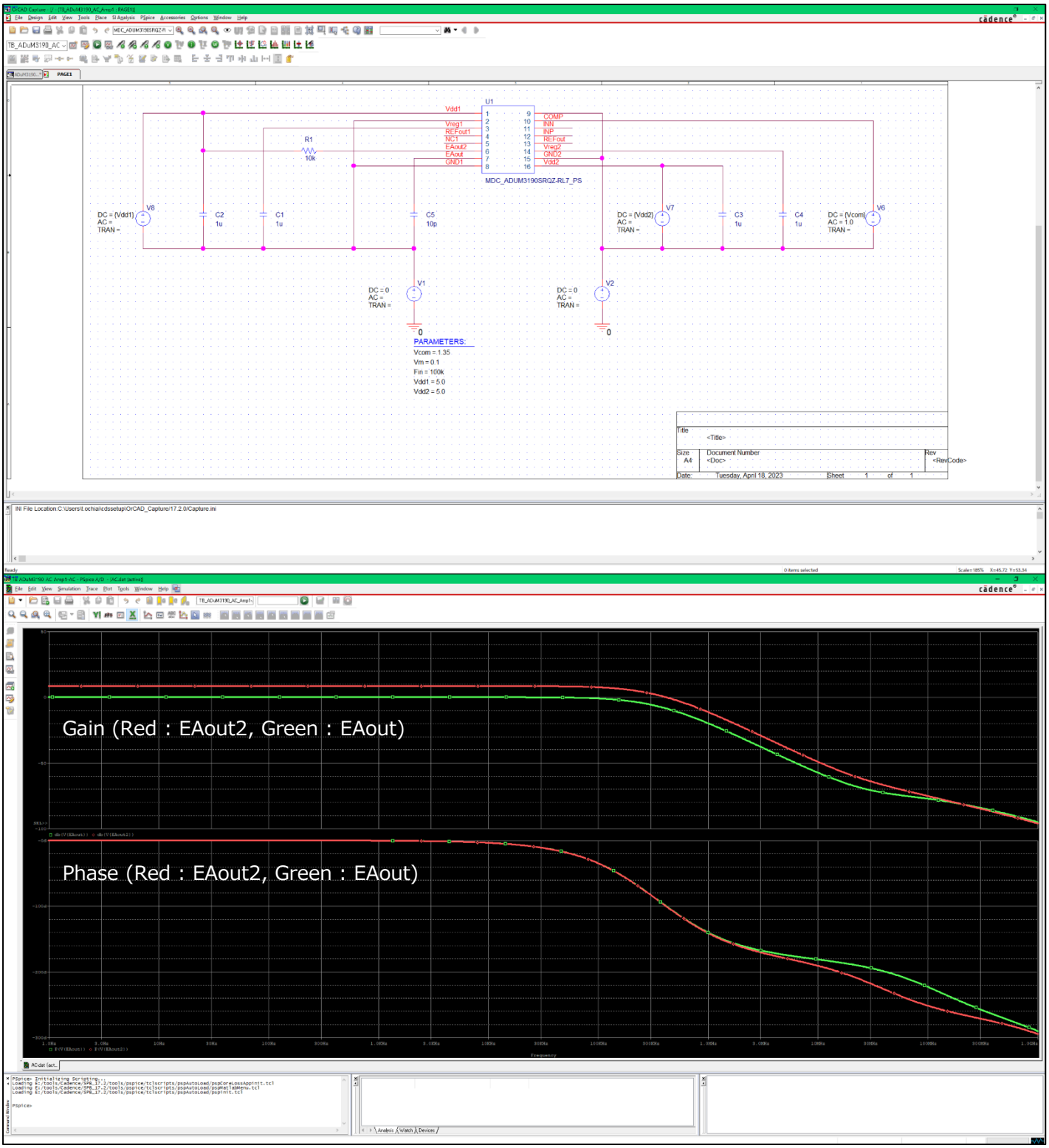
Testbench for transient response of input and output voltage (Vdd1, Vdd2 = 5.0[V], +IN Vm = 100[mV])

Referred to Data Sheet



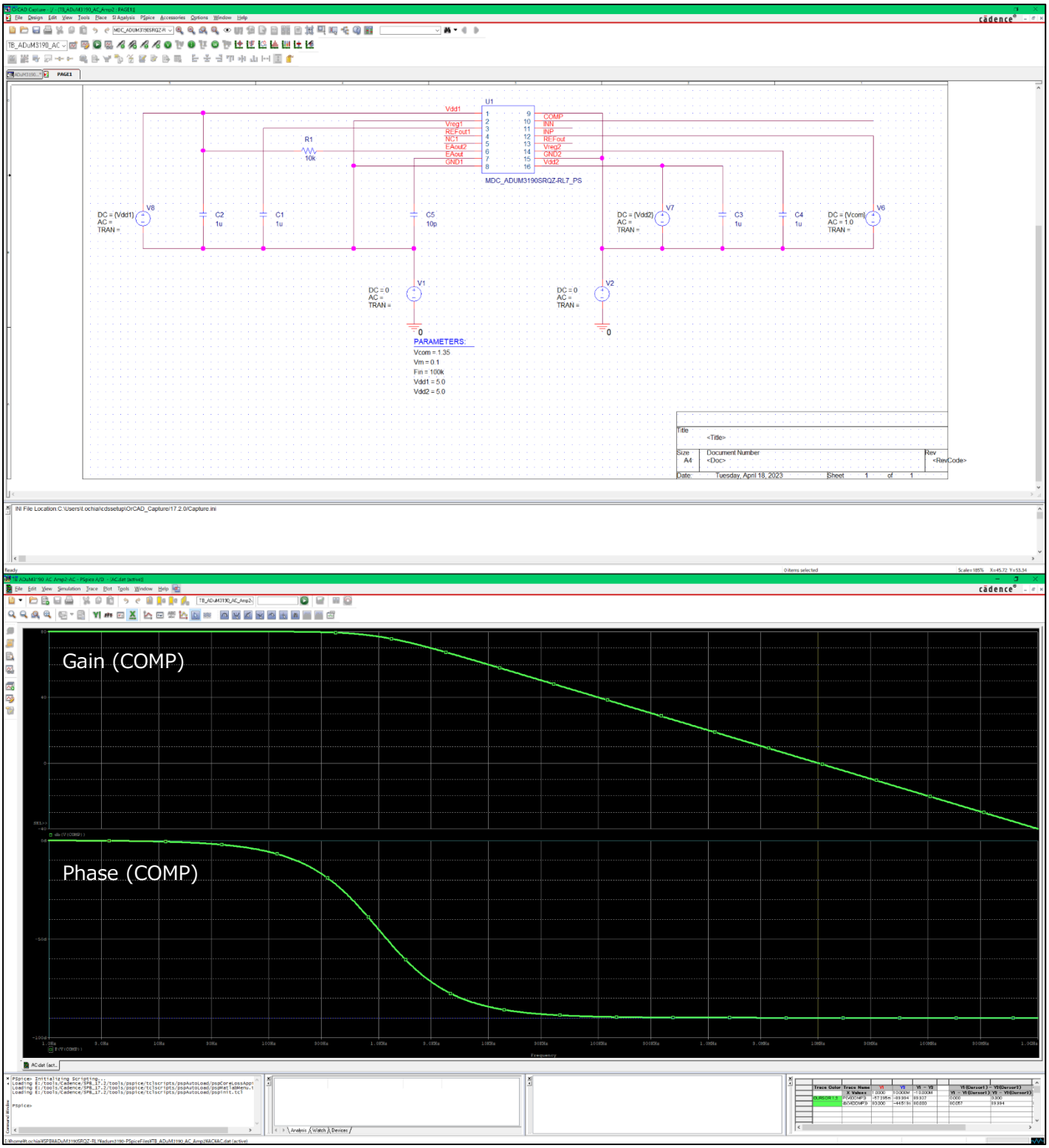
Testbench for frequancy response of Amp.1 (Vdd1, Vdd2 = 5.0[V])

Referred to Data Sheet



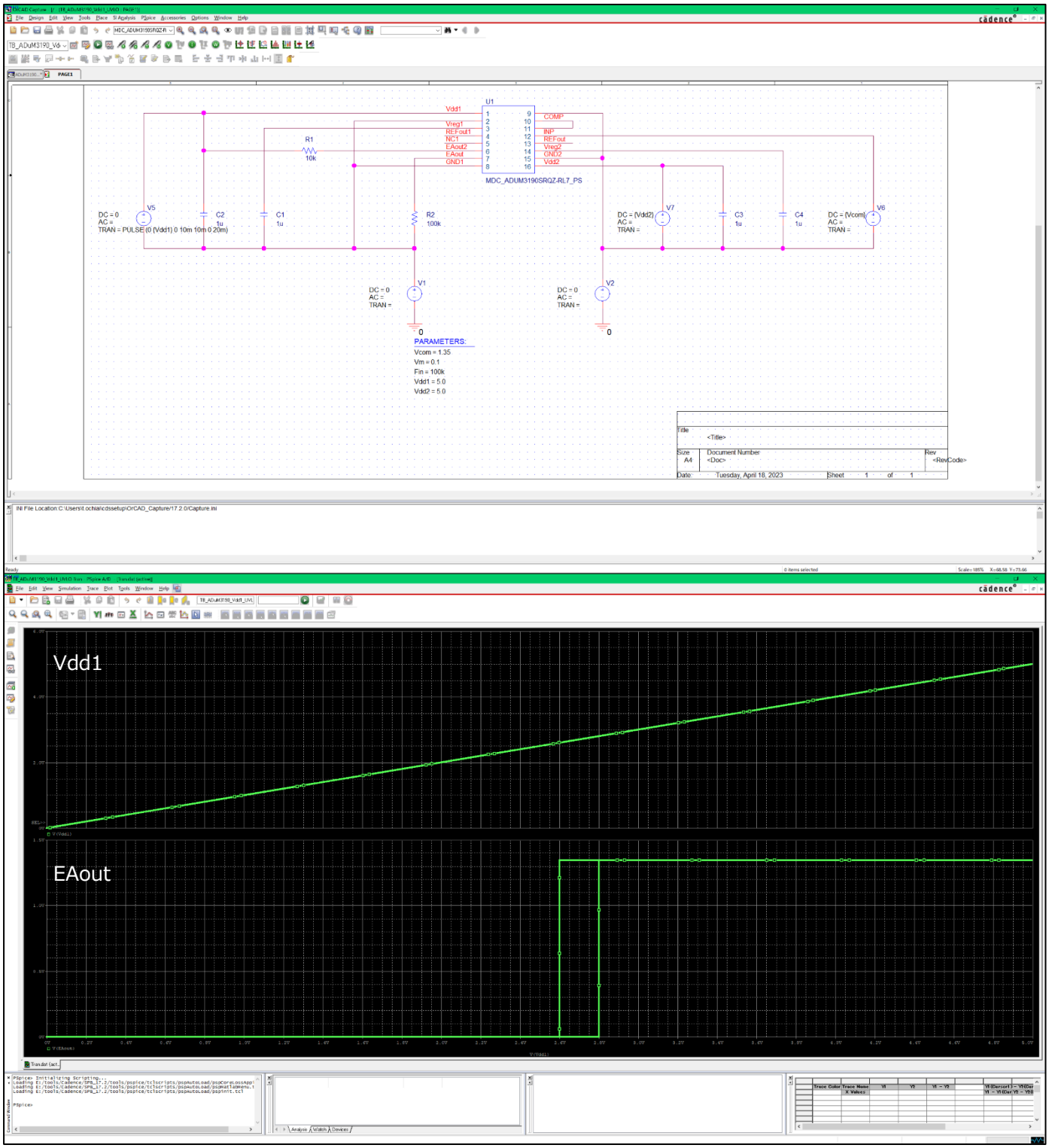
Testbench for frequancy response of Amp.2 (Vdd1, Vdd2 = 5.0[V])

Referred to Data Sheet



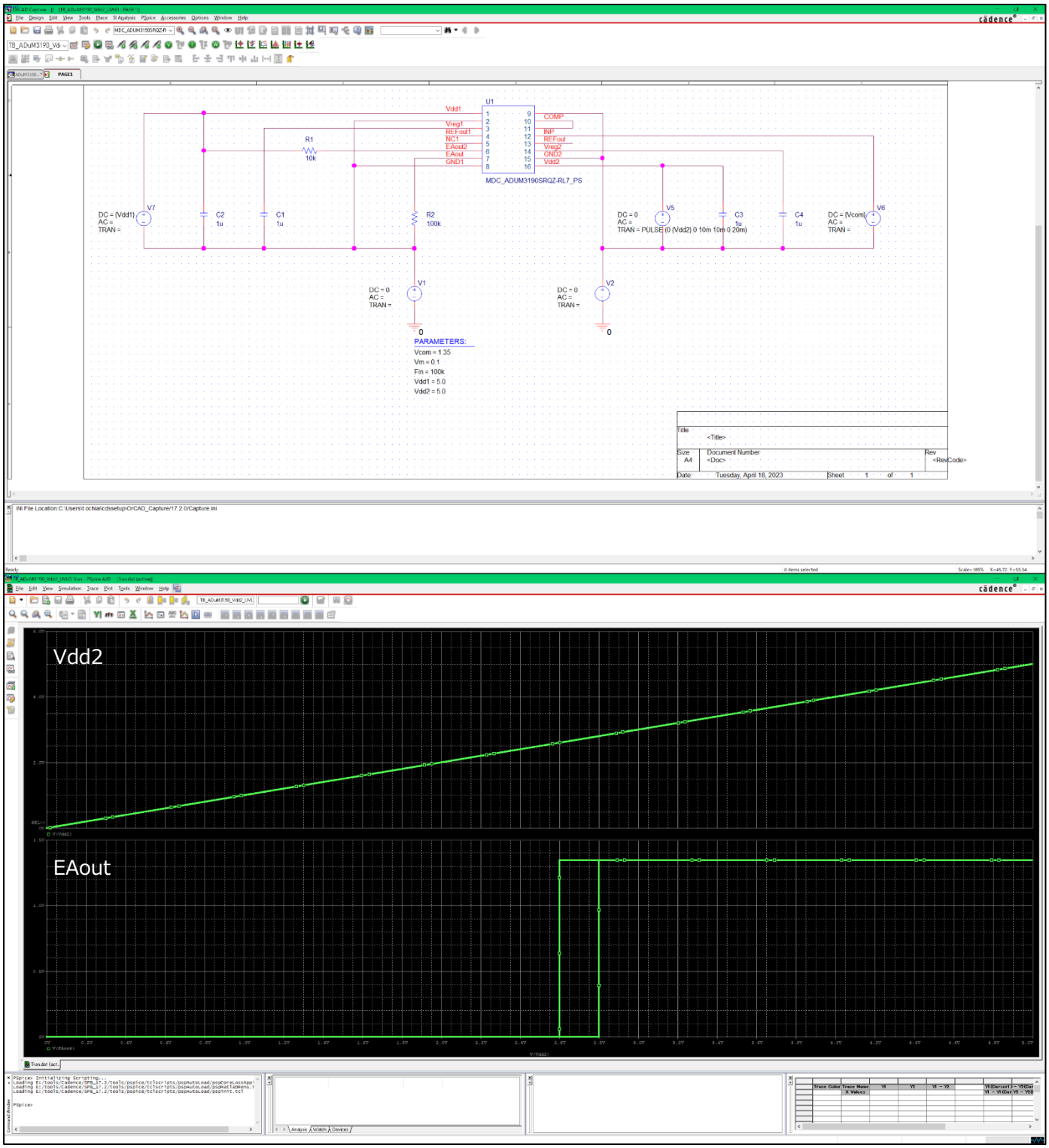
Testbench for Vdd1 UVLO function (Vdd1, Vdd2 = 5.0[V], +IN = 1.35[V])

Referred to Data Sheet



Testbench for Vdd1 UVLO function (Vdd2, Vdd2 = 5.0[V], +IN = 1.35[V])

Referred to Data Sheet



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