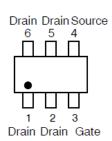
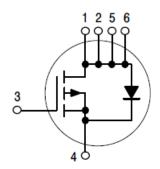


# LTspice Model PMOS ON NTGS3136PT1G

#### PIN ASSIGNMENT





## **Model Information**

Model A macro model based on BSIM3 model

Call Name MDC\_NTGS3136PT1G\_LT Pin Assign 1:D 2:D 3:G 4:S 5:D 6:D

File List Model Library MDC\_NTGS3136PT1G\_LT02.lib

Model Report MDC\_NTGS3136PT1G\_LT.pdf (this file)

**Verified Simulator Version** 

Note

LTspice version XVII

#### References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version
Product name
Company name
May, 2019 Rev. 2
NTGS3136PT1G
ON Semiconductor.

Characteristics IdVds[Vgs],IdVgs[Temp],Rds(on)Vgs[Temp],Rds(on)Id[Vgs],

NormRds(on)Temp[Id],CapacitanceVds[Cname],VgsQg[Vdd],VdsQg[Vdd],IsVsd[Temp],VthTemp[Id],SwitchingIdd[Tname]

,Trrlf[Ir],SwitchingWaveform,TrrWaveform

#### Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-20	V
Gate-source voltage (DC)	8	to	-8	V
Temperature	-55	to	150	deg C



**Model Functions Table** 

# **MOSFET**

O: Implemented

× : Not Implemented

—: Not applicable

# RANK=1

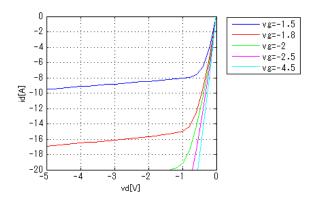
	KANK=1	
Functions	RANK	Implemented
ID-VDS-VGS	1	0
ID-VGS(Temp)	1	0
RDS(on)-VGS-ID	1	_
RDS(on)-VGS-Temp	1	0
RDS(on)-ID-VGS	1	0
RDS(on)-ID-Temp	1	_
RDS(on)-Temp-VGS	1	_
RDS(on)-Temp-ID	1	0
Capacitance	1	0
Gate Charge	1	0
IS-VSD(Forward)	1	0
Reverse recovery	1	0
Switching(Typ.)	1	0
Bv-Temp	1	_
Yfs-ID-Temp	1	_



Simulation results are following. Explanatory notes — : simulated

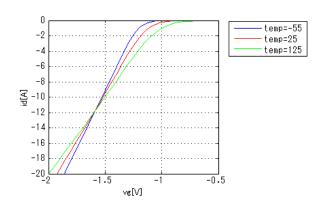
#### IdVds[Vgs]

Temp = 25degC



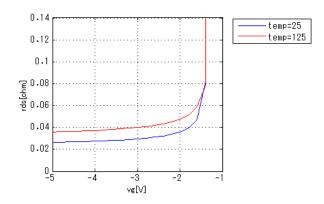
### IdVgs[Temp]

Vds = -5V



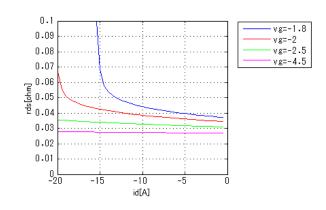
#### Rds(on)Vgs[Temp]

Id = -5.1A



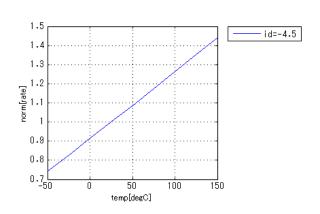
#### Rds(on)Id[Vgs]

Temp = 25degC



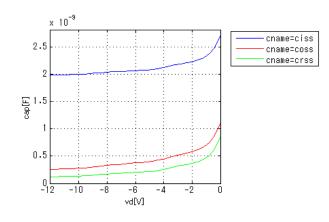
#### NormRds(on)Temp[Id]

Vgs = -5.1V



#### CapacitanceVds[Cname]

freq = 1000000Hz

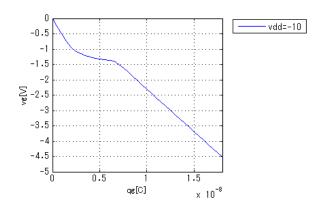




Simulation results are following. Explanatory notes — : simulated

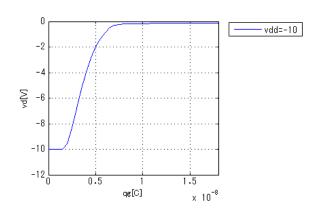
### VgsQg[Vdd]

Id = -5.1A



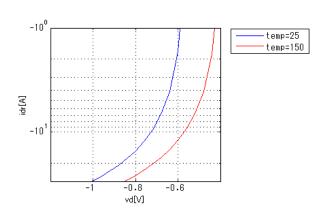
### VdsQg[Vdd]

Id = -5.1A



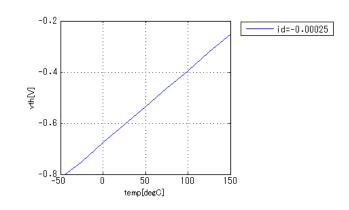
#### IsVsd[Temp]

vg = 0V



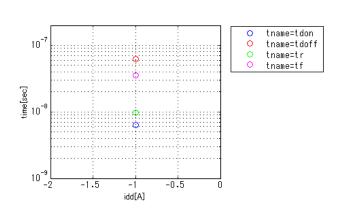
#### VthTemp[Id]

Vd = Vg



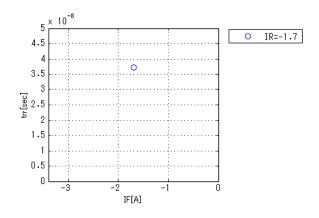
#### Switchingldd[Tname]

vgg = -4.5V, vdd = -10V, RGG = 60hm



#### Trrlf[lr]

vdd = -5V, didt = 100A/us, Temp = 25degC

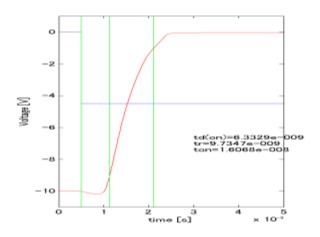


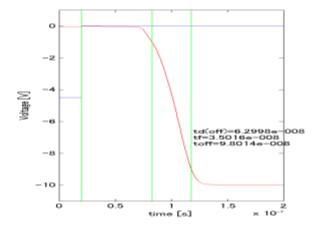


Simulation results are following. Explanatory notes — : simulated

### Switching Waveform (Blue : INPUT Red : OUTPUT)

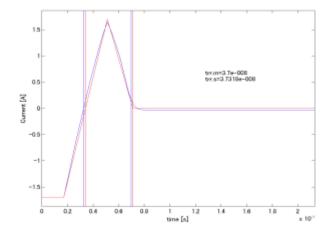
vgg = -4.5V, vdd = -10V, RGG = 60hm, idd = -1A





#### Trr Waveform (Red : Datasheet Blue : Simulation)

vdd = -5V, didt = 100A/us, Temp = 25degC, IF = -1.7A





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MoDeCH Inc.

**Head Office** 

Location: Taiju-Seimei-Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan

Tel:+81-42-656-3360

E-Mail:model-on-support@modech.co.jp

URL:http://www.modech.com/en/

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