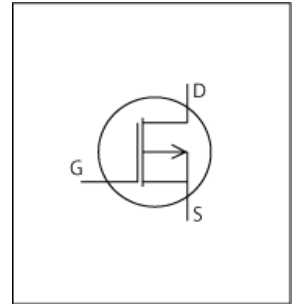


LTspice Model

PMOS

Infineon

SPP18P06P H



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_SPP18P06P_H_LT
Pin Assign 1:G 2:D 3:S
File List Model Library MDC_SPP18P06P_H_LT01.lib
 Model Report MDC_SPP18P06P_H_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev.1.92
- Product name SPP18P06P H
- Company name Infineon Technologies AG
- Characteristics IdVds[Vgs], IdVgs[Temp], Rds(on)Id[Vgs], Rds(on)Temp[Vgs], Crss, Coss, Ciss, VthTemp[Id], VgsQg[Vdd], IsVsd[Temp], tdon, tdoft, tf, tr

Simulation Range

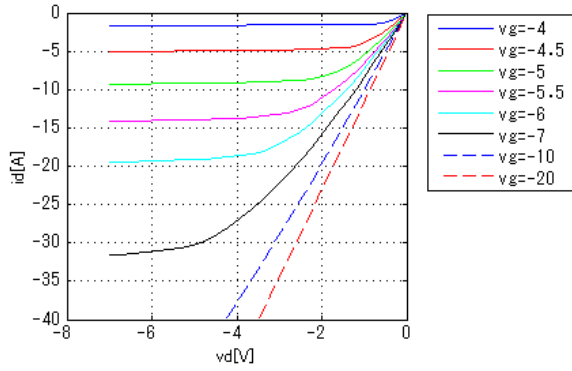
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-60	V
Gate-source voltage (DC)	0	to	-20	V
Temperature	-55	to	175	deg C

Simulation results are following.
 Explanatory notes — : simulated

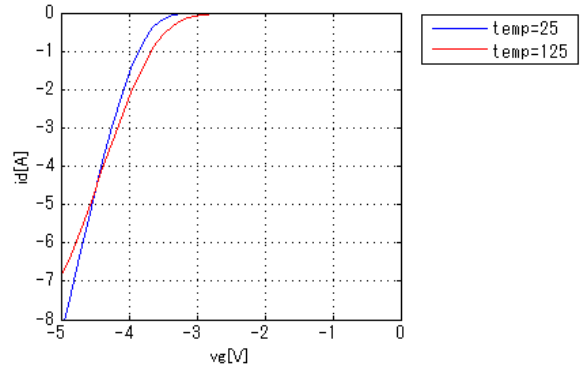
IdVds[Vgs]

Temp. = 25deg C

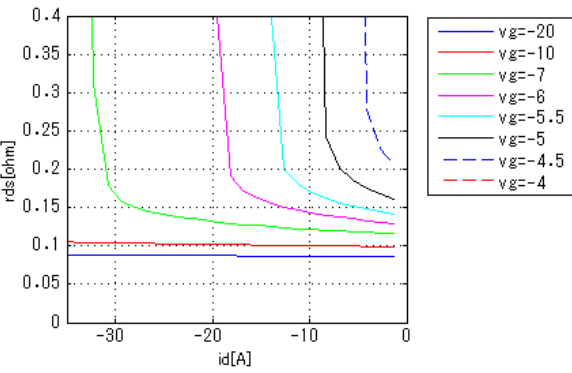


IdVgs[Temp]

Vds = -2V

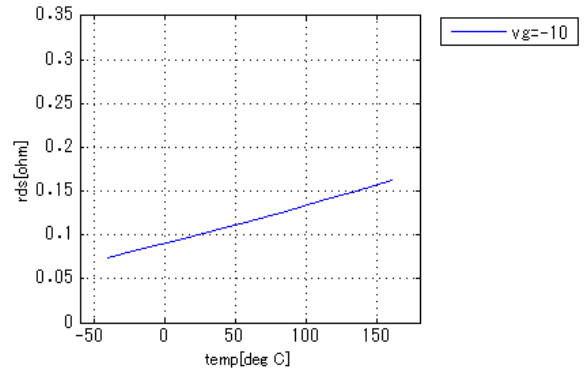


Rds(on)Id[Vgs]



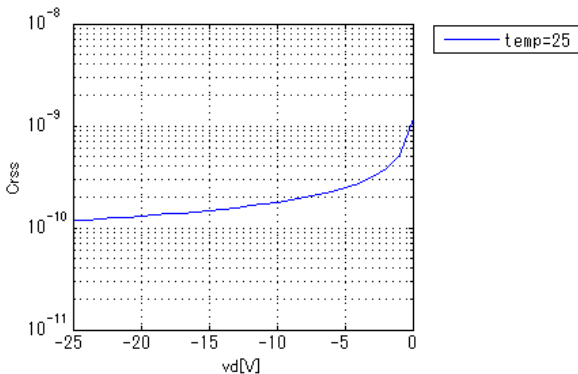
Rds(on)Temp[Vgs]

Id = -13.2A



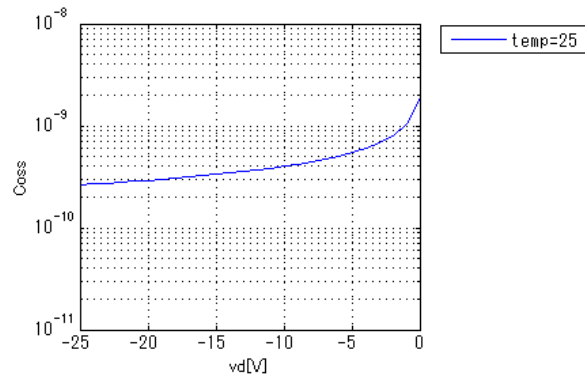
Crss

Freq. = 1MHz



Coss

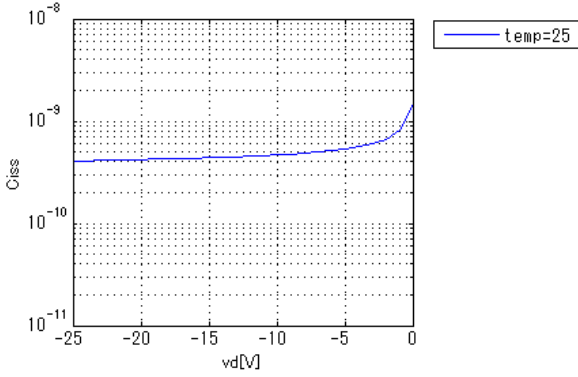
Freq. = 1MHz



Simulation results are following.
 Explanatory notes — : simulated

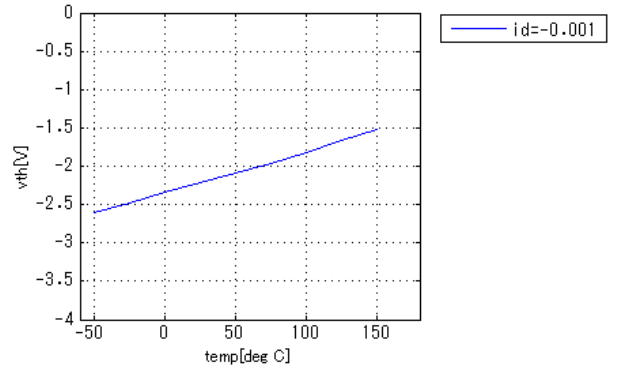
Ciss

Freq. = 1MHz



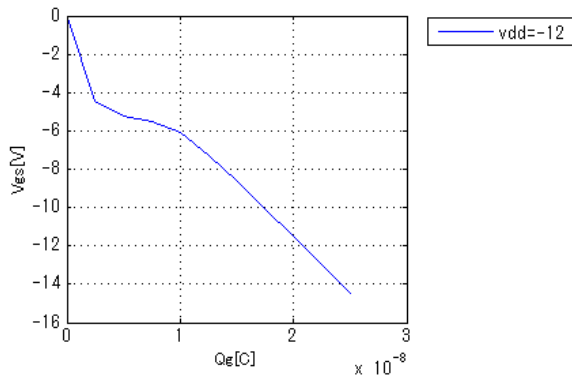
VthTemp[Id]

Vd = Vg



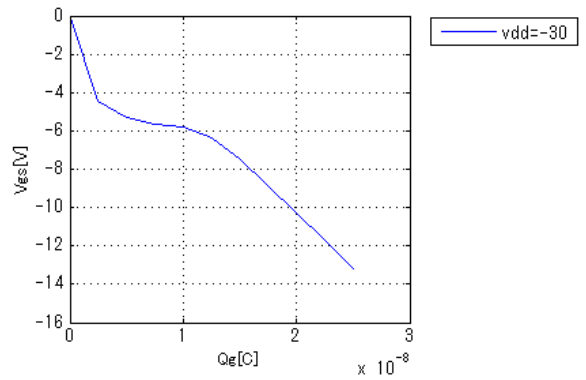
VgsQg[Vdd]

Id = -18.6A



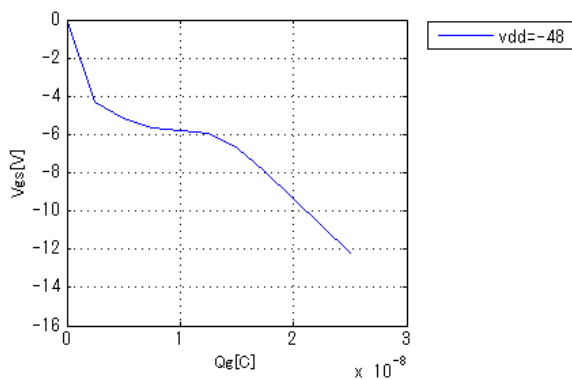
VgsQg[Vdd]

Id = -18.6A

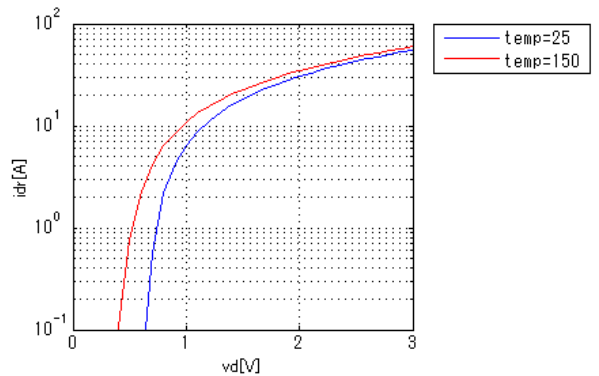


VgsQg[Vdd]

Id = -18.6A



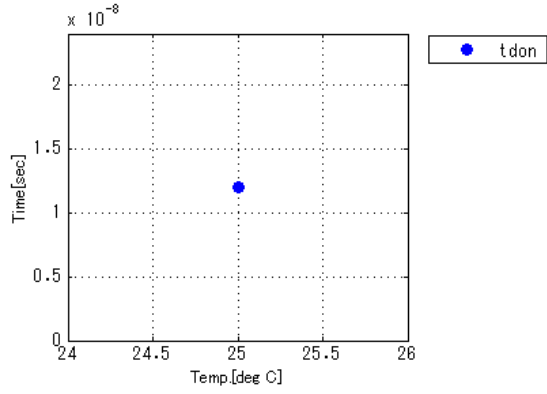
IsVsd[Temp]



Simulation results are following.
 Explanatory notes — : simulated

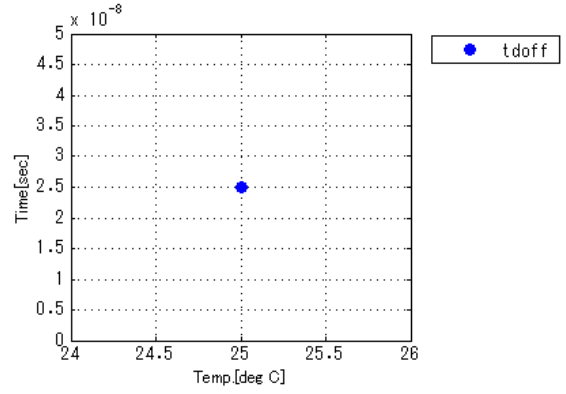
tdon

Vdd = -30V, Id = -13.2A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



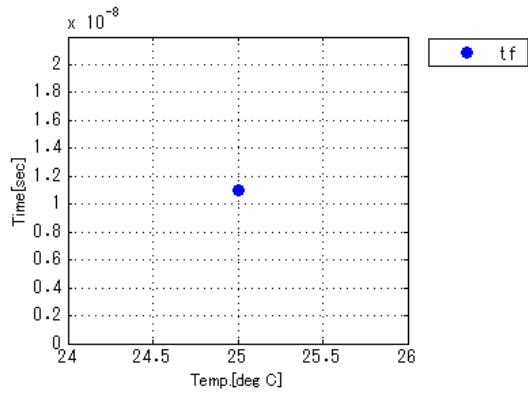
tdoff

Vdd = -30V, Id = -13.2A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



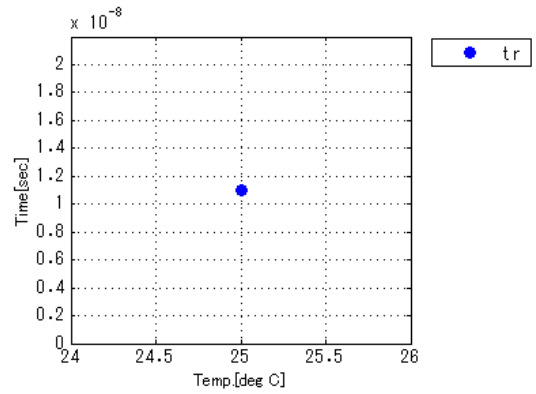
tf

Vdd = -30V, Id = -13.2A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



tr

Vdd = -30V, Id = -13.2A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



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