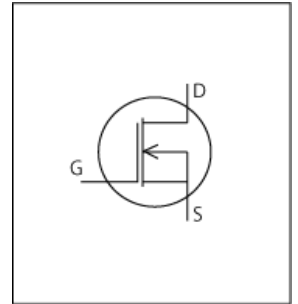


# PSpice Model

## NMOS

### FUJI ELECTRIC

### 2SK3273-01MR



#### Model Information

**Model** A macro model based on BSIM3  
**Call Name** MDC\_2SK3273-01MR\_PS  
**Pin Assign** 1:D 2:G 3:S  
**File List** Model Library MDC\_2SK3273-01MR\_PS01.lib  
 Model Report MDC\_2SK3273-01MR\_PS.pdf (this file)

**Verified Simulator Version** PSpice version 16.6  
**Note**

#### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Unknown
- Product name 2SK3273-01MR
- Company name FUJI ELECTRIC CO., LTD.
- Characteristics IdVgs[Temp], IdVds[Vgs], Crss, Coss, Ciss, Rds(on) Id[Vgs], Rds(on) Temp[Id], VthTemp[Id], VdsQg[Vdd], VgsQg[Vdd]

#### Simulation Range

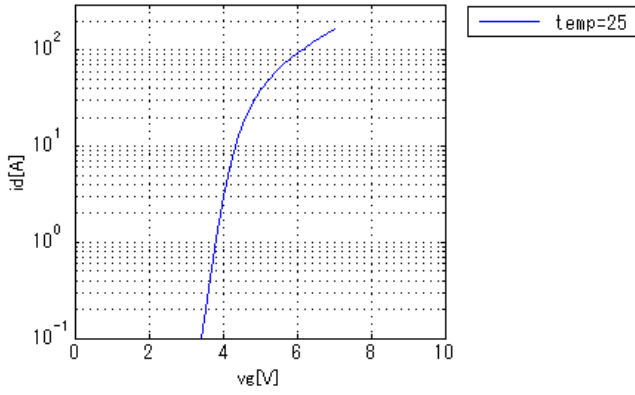
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	0	to	30	V
Temperature	-55	to	150	deg C

Simulation results are following.  
 Explanatory notes — : simulated

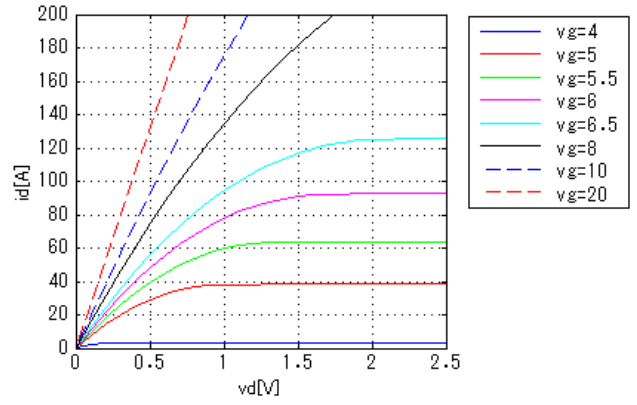
**IdVgs[Temp]**

Vds = 10V



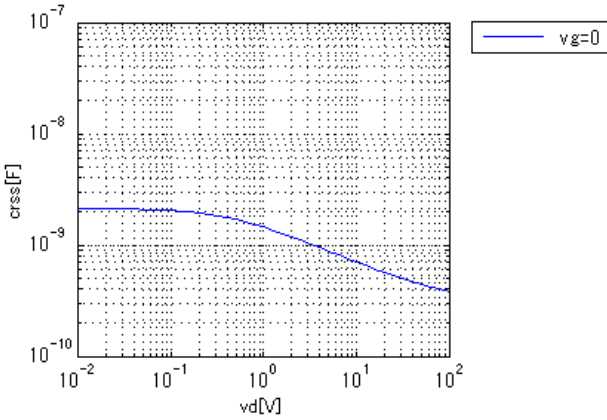
**IdVds[Vgs]**

Temp. = 25deg C



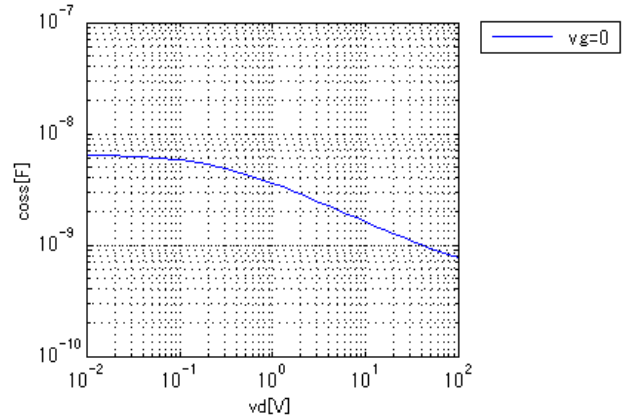
**Crss**

Freq. = 1MHz



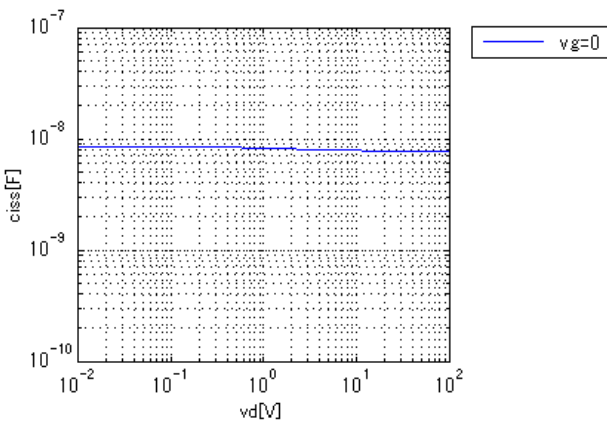
**Coss**

Freq. = 1MHz

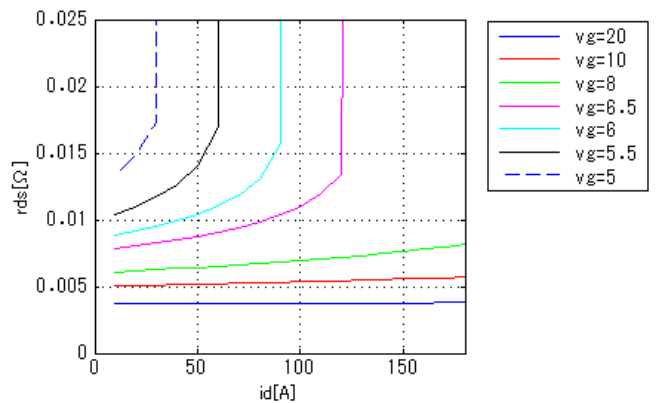


**Ciss**

Freq. = 1MHz

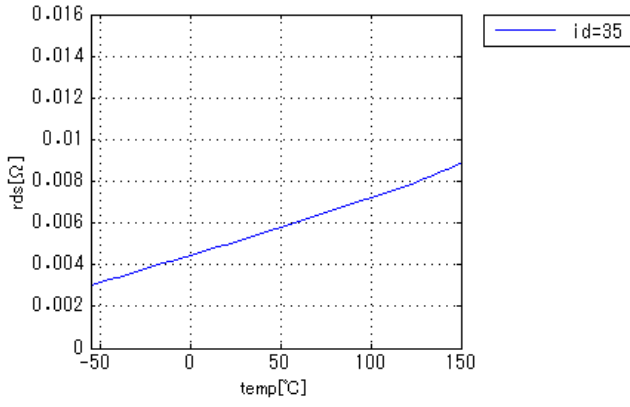


**Rds(on)Id[Vgs]**

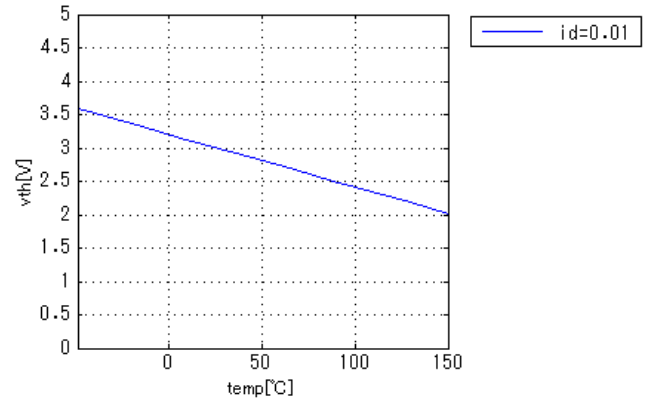


Simulation results are following.  
 Explanatory notes — : simulated

**Rds(on)Temp[Id]**

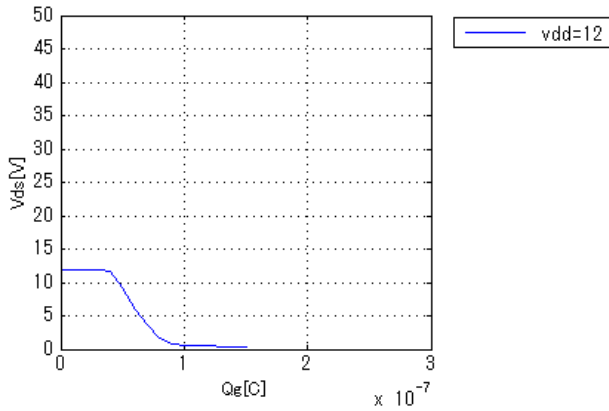


**VthTemp[Id]**



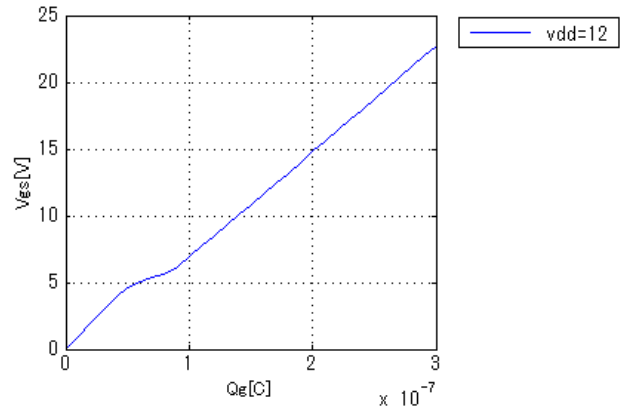
**VdsQg[Vdd]**

Id = 80A



**VgsQg[Vdd]**

Id = 80A



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