

LTspice Model Dual Comparator Texas Instruments Inc. TLV7256IDDUR

Model Information

Model	A macro model		
Call Name	MDC_TLV7256IDDUR_LT		
Pin Assign	1:10UT 2:1IN-	3:1IN+ 4:VCC- 5:2IN+ 6:2IN- 7:2OUT 8:VCC+	
File List	Model Library	MDC_TLV7256IDDUR_LT01.lib	
	Model Report	MDC_TLV7256IDDUR_LT.pdf(this file)	
Verified Simulator Version		LTspice XVII	

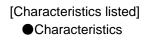
Note

References

The information which was used for modeling is as follow:

[Data Sheet] ●Date/Version ●Product name ●Company name

10-Dec-2020 TLV7256IDDUR Texas Instruments Inc.



Vio,lio,lcc,lsink,lsource,Vol,Voh tpLH,tpHL,tTLH,tTHL

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

ltem	Min	Тур	Max	Unit
VDD	1.5		7.0	V
Temperature		25		deg C

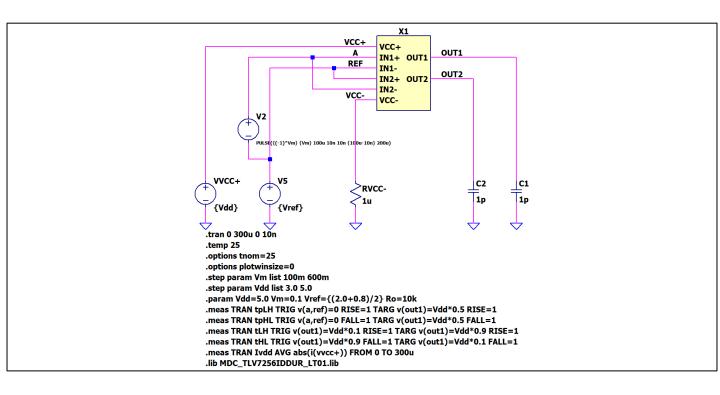


Model Functions Table

Functions	Implemented
Low supply current: IDD = 20μA (typ.)	0
Single power supply	0
Rail-to-Rail Common-Mode Input Voltage Range	0
Push-Pull Output Circuit	0
Low Input-Bias Current	0



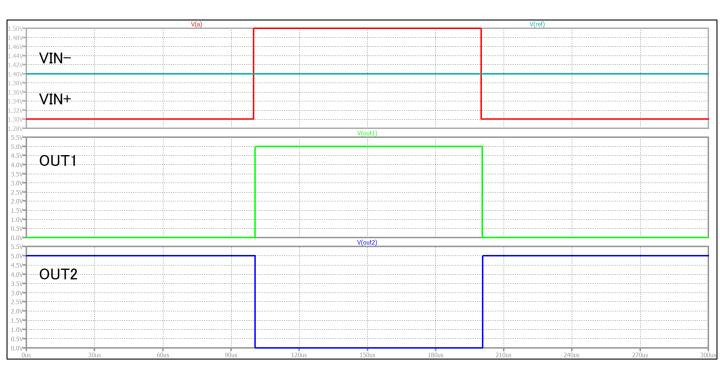
Testbench for transient characteristics (Vcc+=5.0[V]/2.7[V]/1.8[V] Vcc-=0.0[V] Vin=+/-100[mV]) Referred to Data Sheet





Simulation results are following. Explanatory notes — : simulated

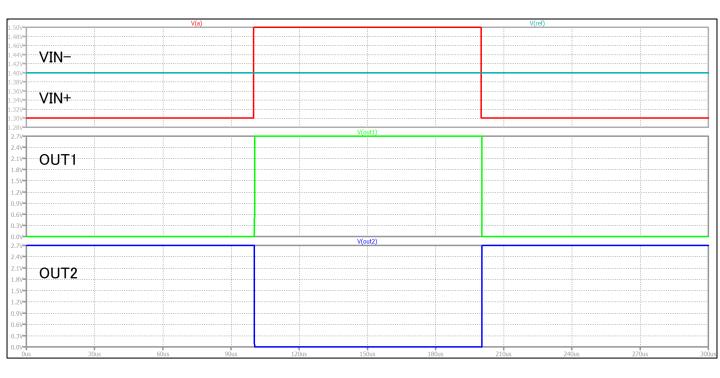
transient characteristics (Vdd=5.0[V] Vss=0.0[V] Vin=+/-100[mV])





Simulation results are following. Explanatory notes — : simulated

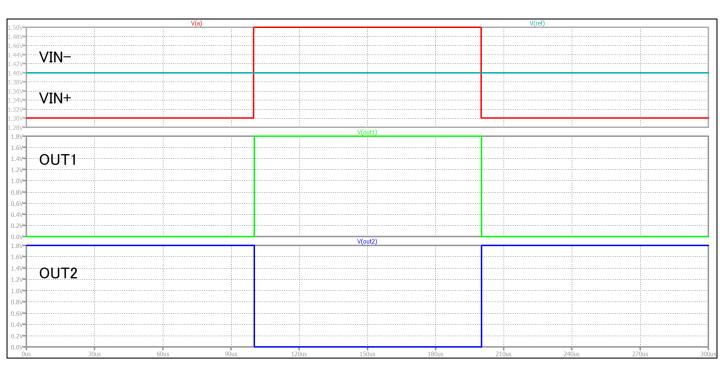
transient characteristics (Vdd=2.7[V] Vss=0.0[V] Vin=+/-100[mV])





Simulation results are following. Explanatory notes — : simulated

transient characteristics (Vdd=1.8[V] Vss=0.0[V] Vin=+/-100[mV])





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