PSpice Model
High-side driver with MultiSense analog feedback for automotive applications STMicroelectronics VN7020AJ

Model Information

Model	A macro model
Call Name	MDC_VN7020AJ_PS
Pin Assign	1:INPUT 2:FaultRSTB 3:SEn 4:AGND 5:SEL0 6:SEL1 7:MultiSense 8:NC1 9:NC2 10:NC3 11:NC4 12:NC5 13:OUTPUT1 14:OUTPUT2 15:OUTPUT3 16:OUTPUT4 17:VCC
File List	Model Library MDC_VN7020AJ_PS01.lib Model Report MDC_VN7020AJ_PS.pdf(this file)

Verified Simulator Version PSpice

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version Rev 4
- ●Product name VN7020AJ
- ●Company name STMicroelectronics

[Characteristics listed]

- ●Characteristics
  - Standby mode activation
  - Normal mode operation
  - Short-circuit condition(Outputs configured for Latch-off)
  - UVLO
  - OFF-state diagnostics (Short to VCC)
  - OFF-state diagnostics (Open-load)
  - Negative output voltage (inductive loads turn-off)
  - Turn-on/Turn-off delay time
  - MultiSense timings (current sense mode)
  - Multisense timings (chip temperature and VCC sense mode)
  - Logic inputs (VIH=1.8V、VIL=1.35V)

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

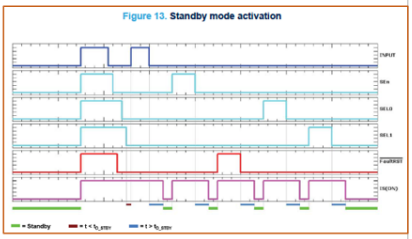
○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table

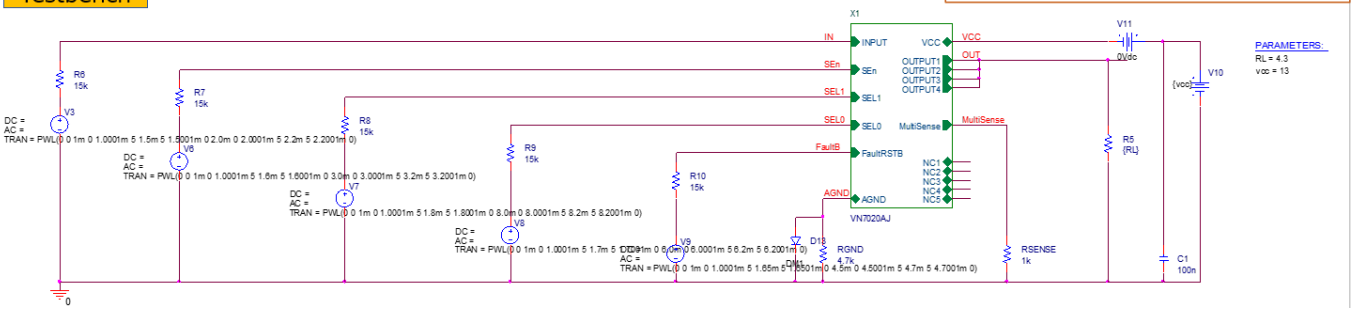
	RANK=1	
Functions	RANK	Implemented
Standby mode activation	1	○
Normal mode operation	1	○
Short-circuit condition(Outputs configured for Latch-off)	1	○
UVLO	1	○
OFF-state diagnostics (Short to VCC)	1	○
OFF-state diagnostics (Open-load)	1	○
Negative output voltage (inductive loads turn-off)	1	○
Turn-on/Turn-off delay time	1	○
MultiSense timings (current sense mode)	1	○
Multisense timings (chip temperature and VCC sense mode)	1	○
Logic inputs (VIH=1.8V、VIL=1.35V)	1	○

Standby mode activation

Simulation results are following.
Explanatory notes — : simulated



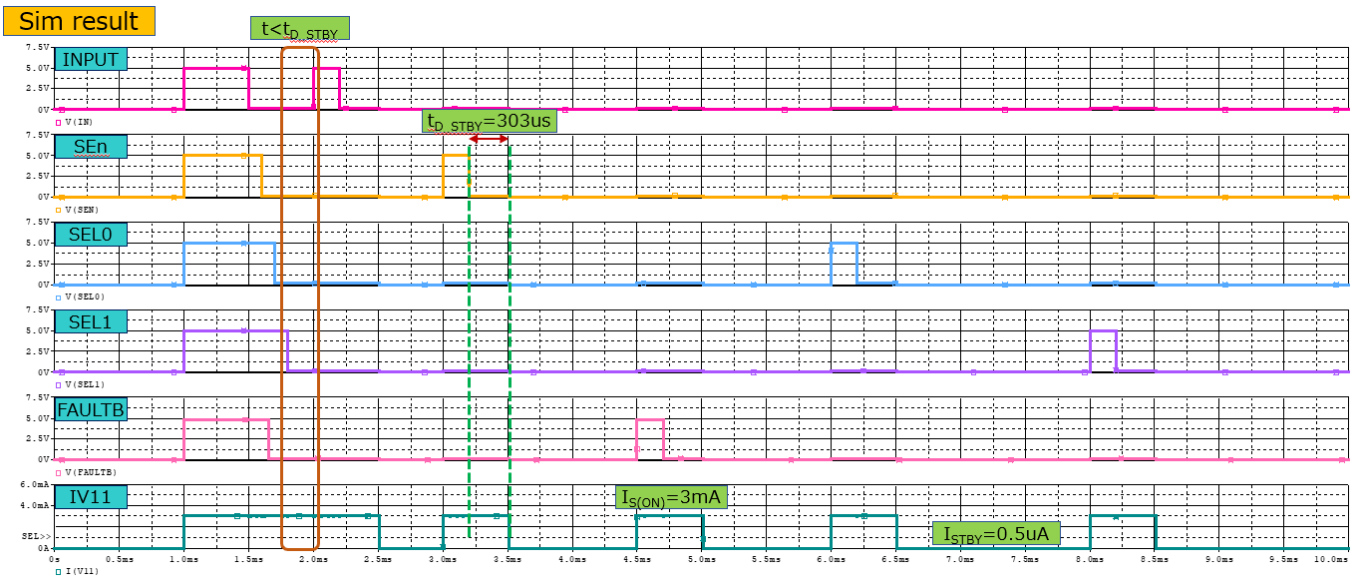
Testbench



Standby mode activation

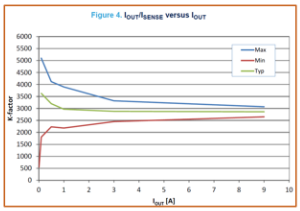
Simulation results are following.
Explanatory notes — : simulated

Sim result

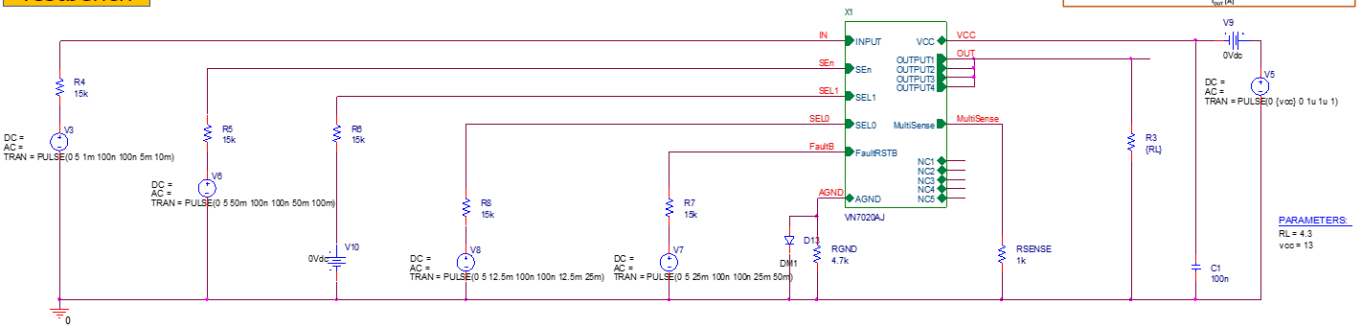


Normal mode operation

Simulation results are following.
Explanatory notes — : simulated



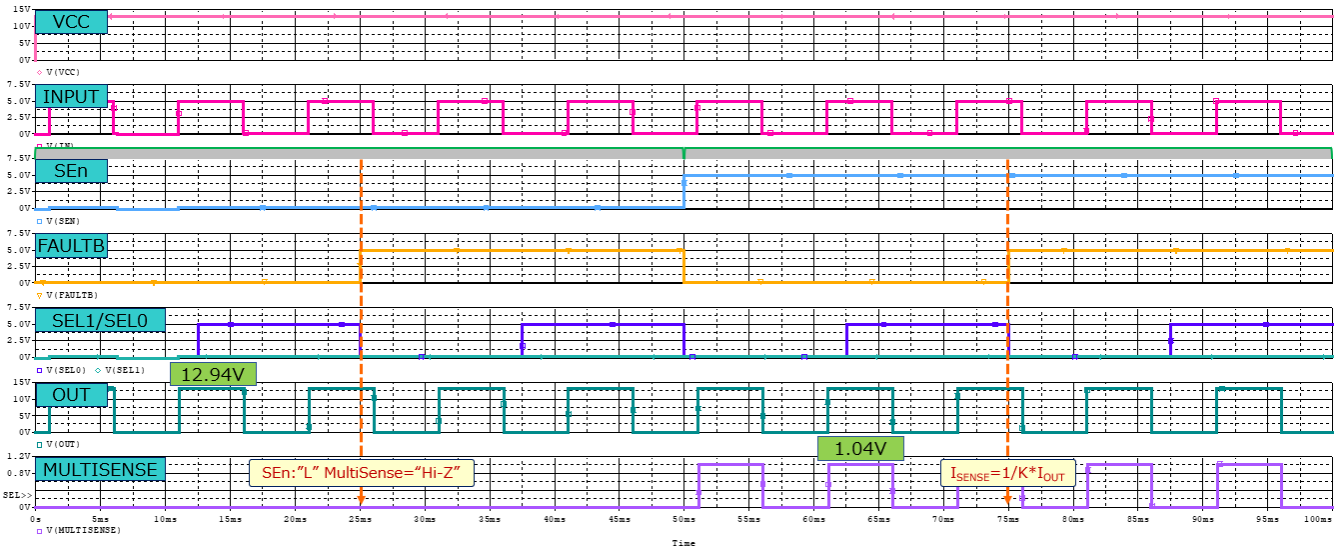
Testbench



Normal mode operation

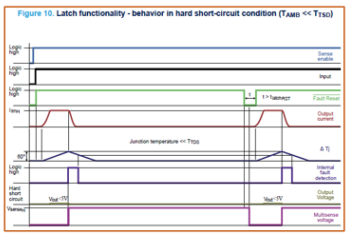
Simulation results are following.
Explanatory notes — : simulated

Sim result

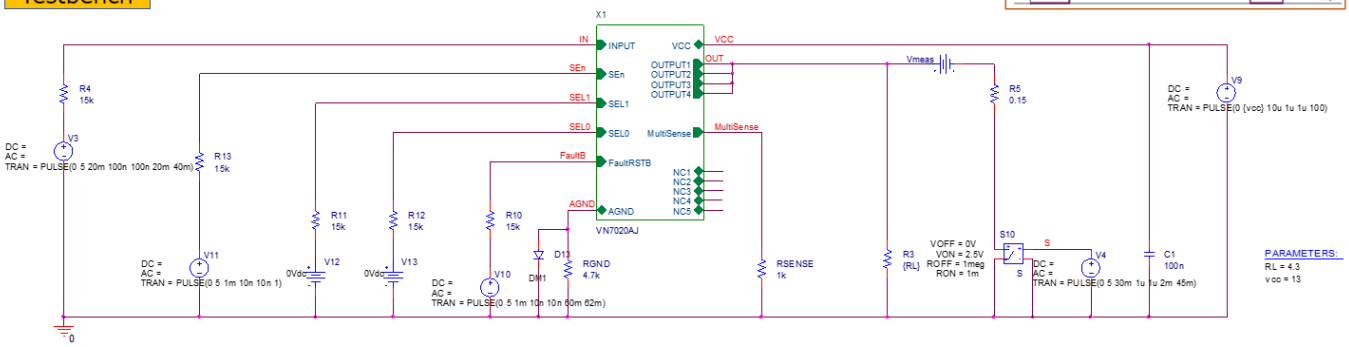


Short-circuit condition(Outputs configured for Latch-off)

Simulation results are following.
Explanatory notes — : simulated



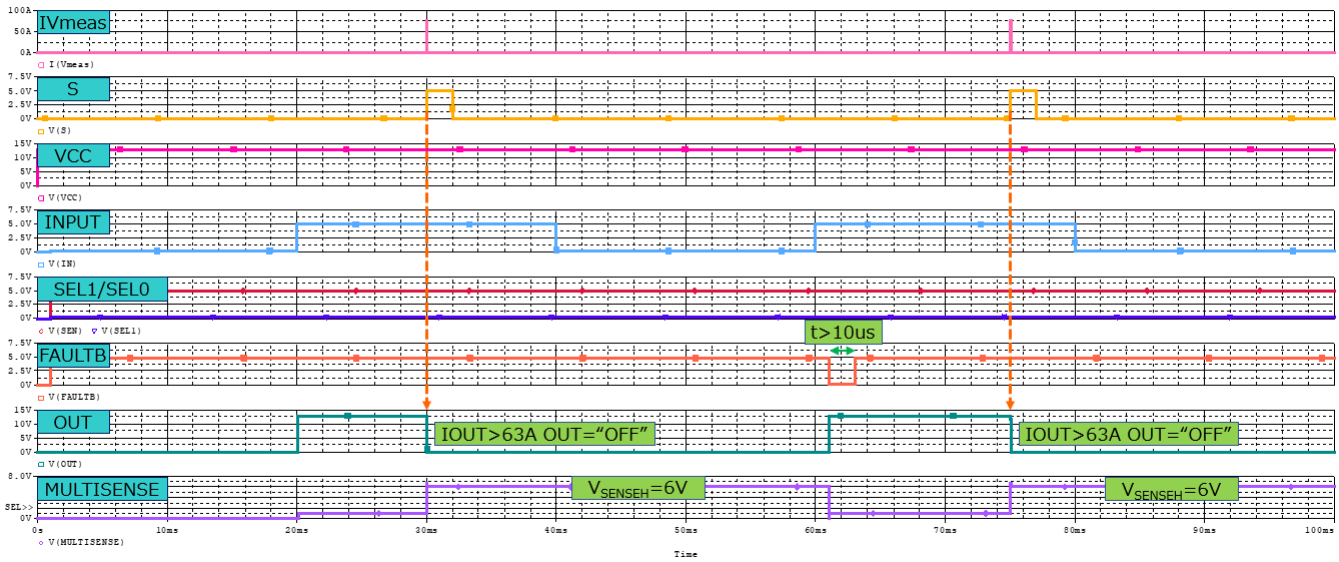
Testbench



Short-circuit condition(Outputs configured for Latch-off)

Simulation results are following.
Explanatory notes — : simulated

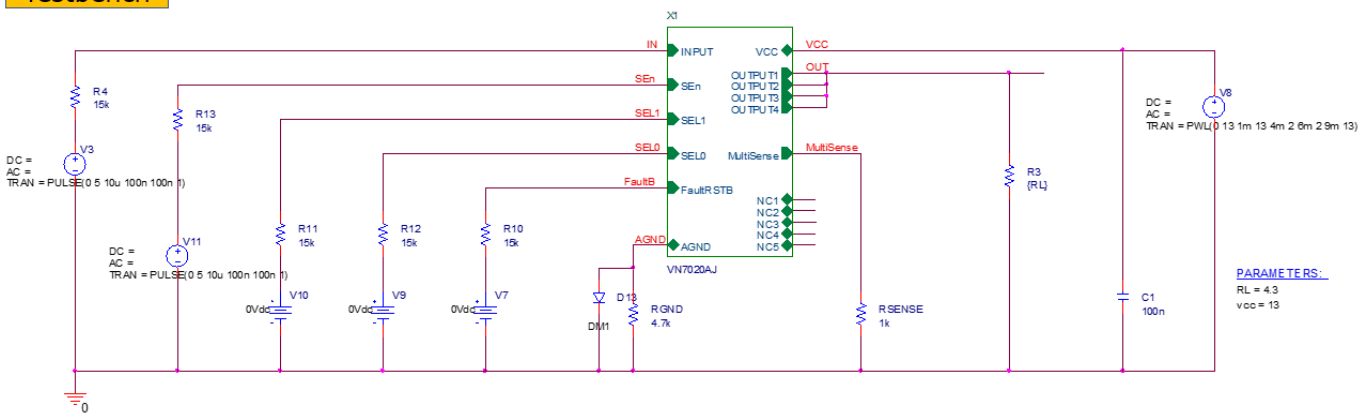
Sim result



UVLO

Simulation results are following.
Explanatory notes — : simulated

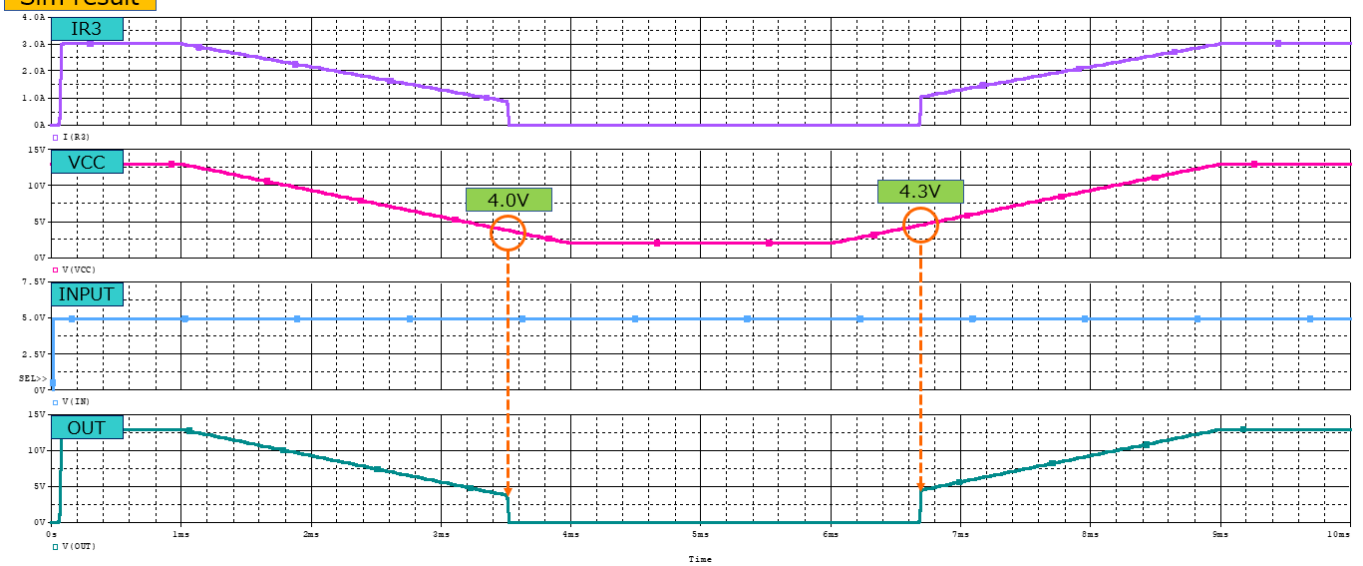
Testbench



UVLO

Simulation results are following.
Explanatory notes — : simulated

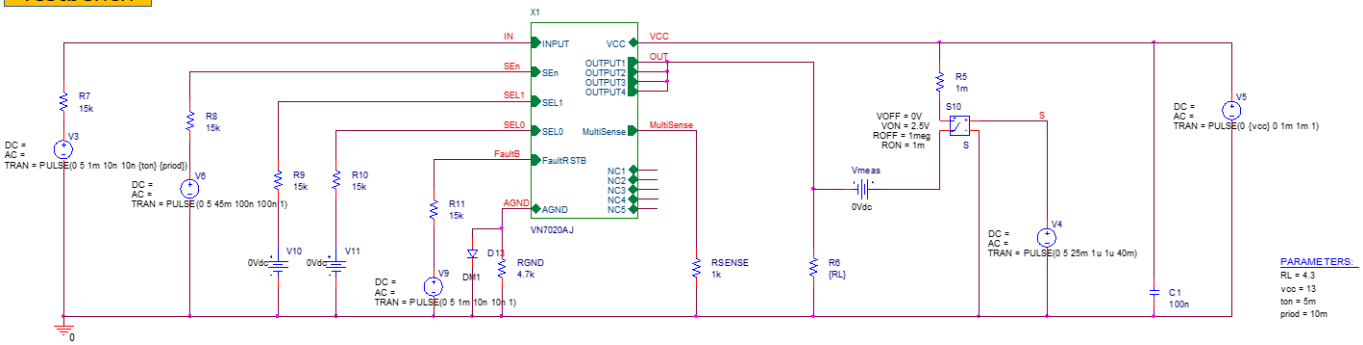
Sim result



OFF-state diagnostics (Short to VCC)

Simulation results are following.
Explanatory notes — : simulated

Testbench

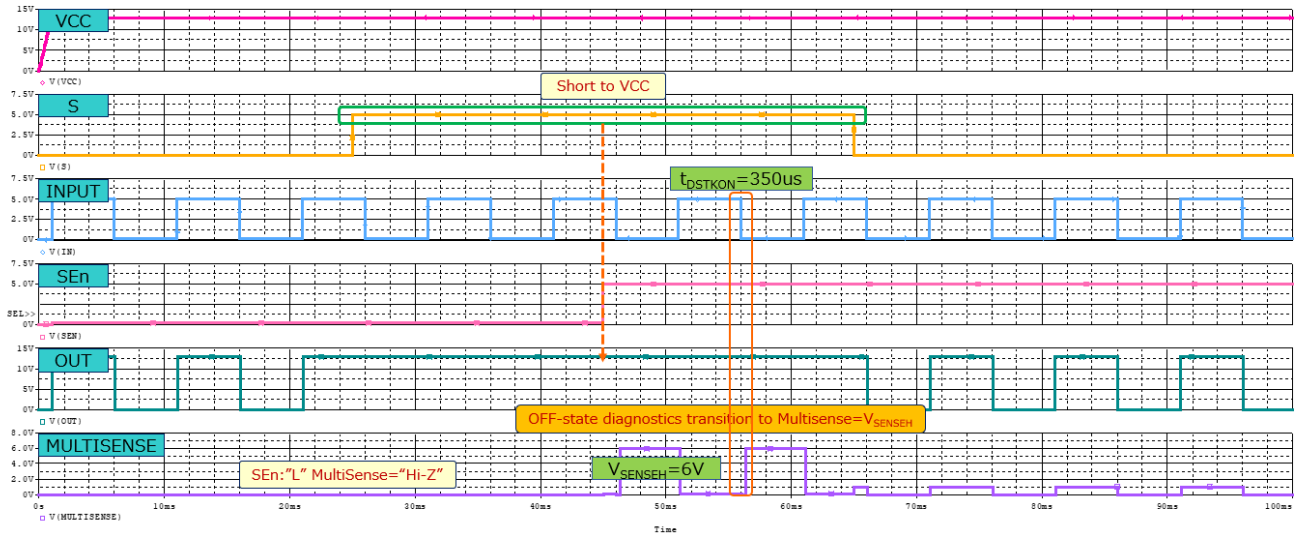


OFF-state diagnostics (Short to VCC)

Simulation results are following.
Explanatory notes — : simulated

	t_{DSTKON}
Data sheet	350us
Sim	350us

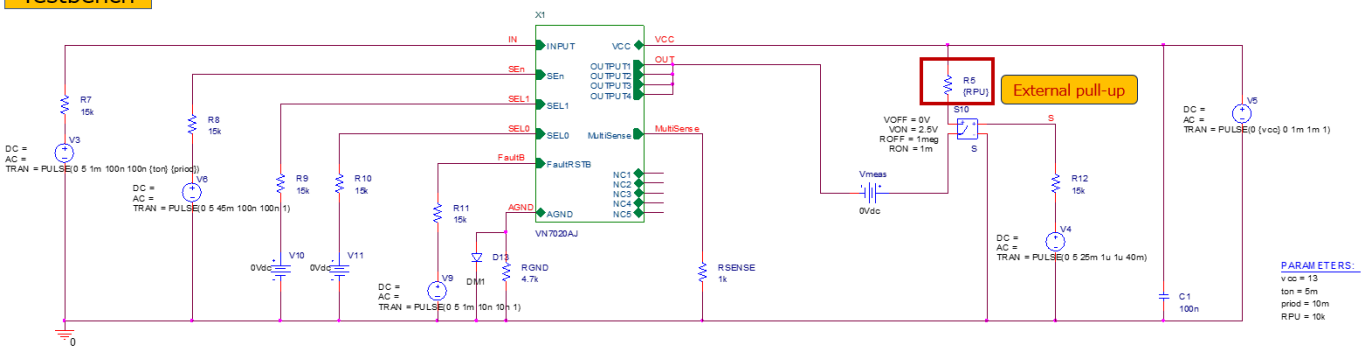
Sim result



OFF-state diagnostics (Open-load)

Simulation results are following.
Explanatory notes — : simulated

Testbench

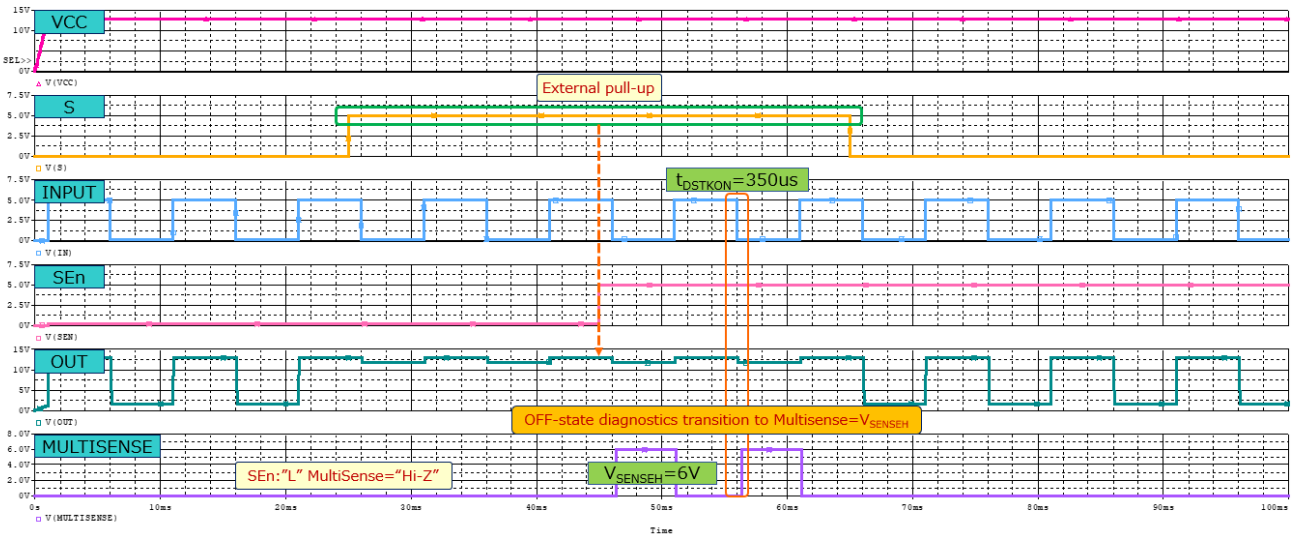


OFF-state diagnostics (Open-load)

Simulation results are following.
Explanatory notes — : simulated

	t_{DSTKON}
Data sheet	350us
Sim	350us

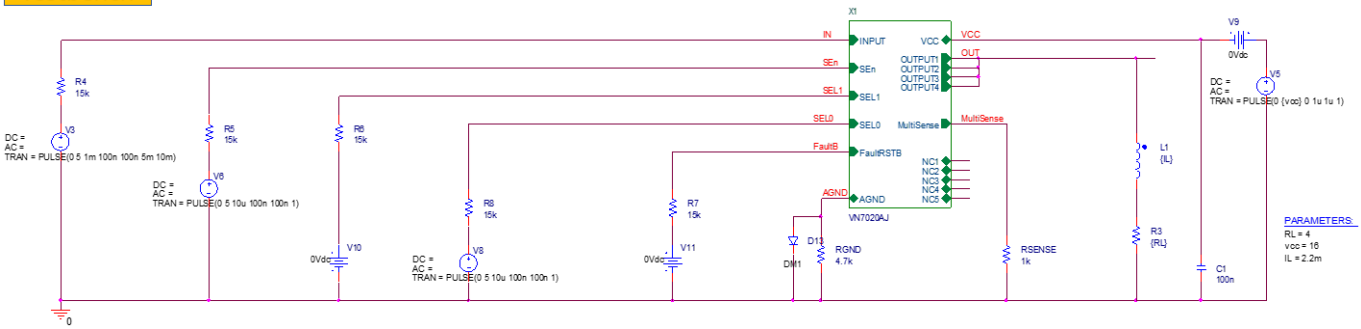
Sim result



Negative output voltage (inductive loads turn-off)

Simulation results are following.
Explanatory notes — : simulated

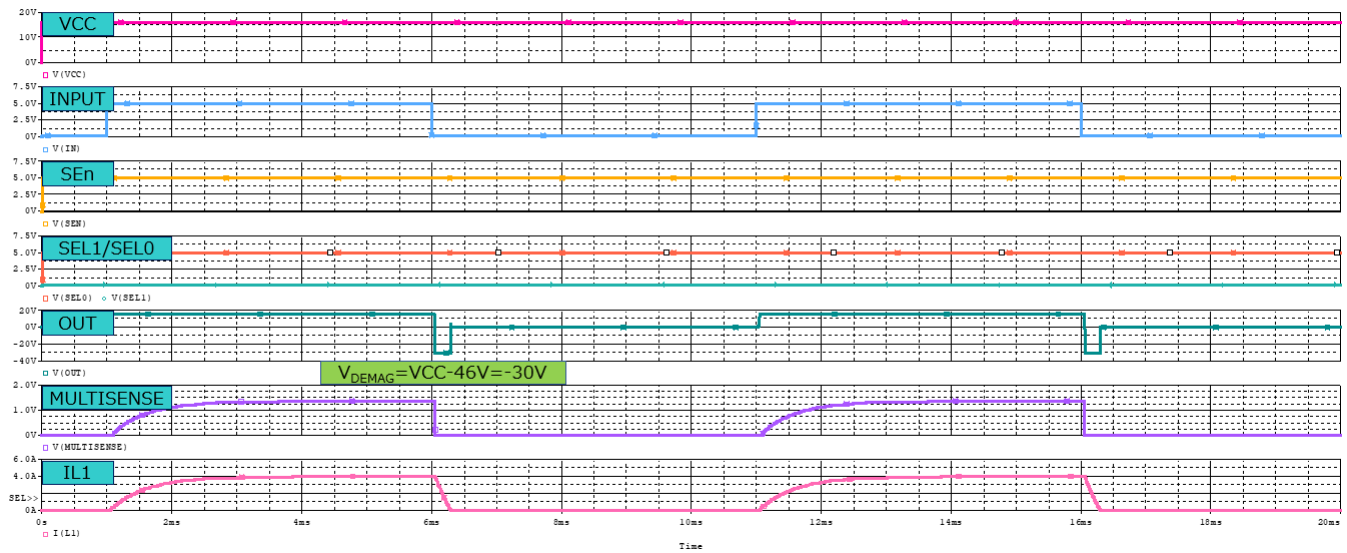
Testbench



Negative output voltage (inductive loads turn-off)

Simulation results are following.
Explanatory notes — : simulated

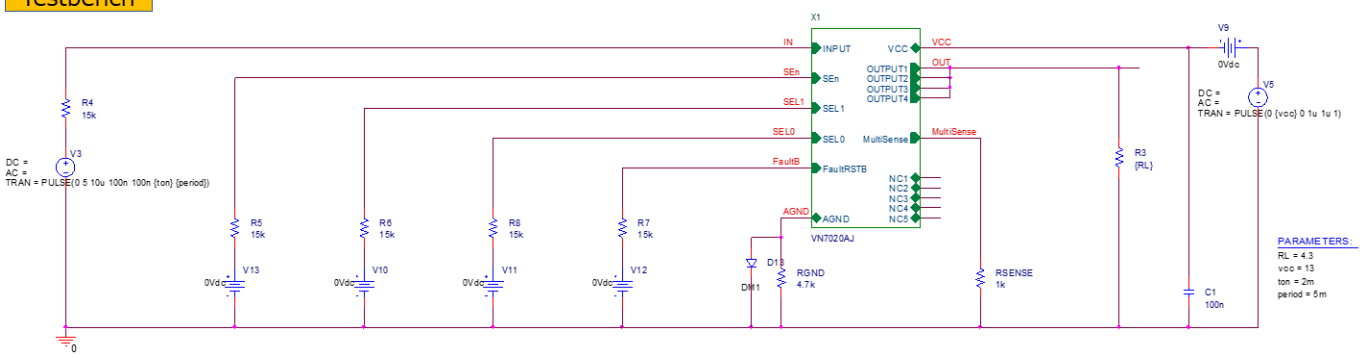
Sim result



Turn-on/Turn-off delay time

Simulation results are following.
Explanatory notes — : simulated

Testbench

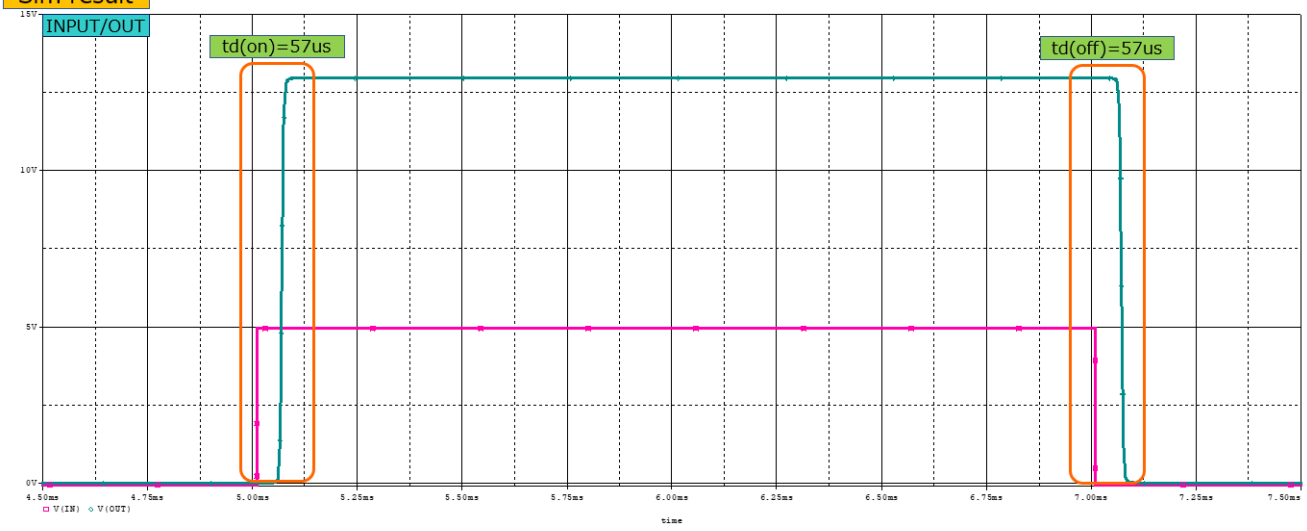


Turn-on/Turn-off delay time

Simulation results are following.
Explanatory notes — : simulated

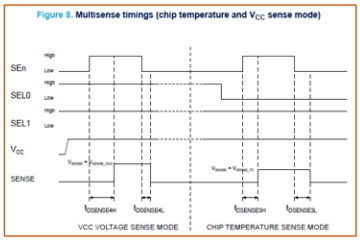
	$t_{d(on)}$	$t_{d(off)}$
Data sheet	60us	40us
Sim	57us	57us

Sim result

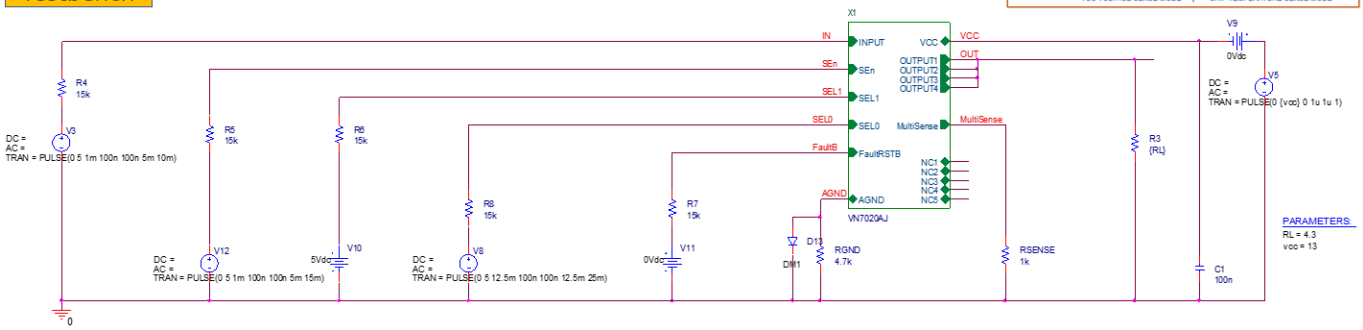


Multisense timings (chip temperature and VCC sense mode)

Simulation results are following.
Explanatory notes — : simulated



Testbench

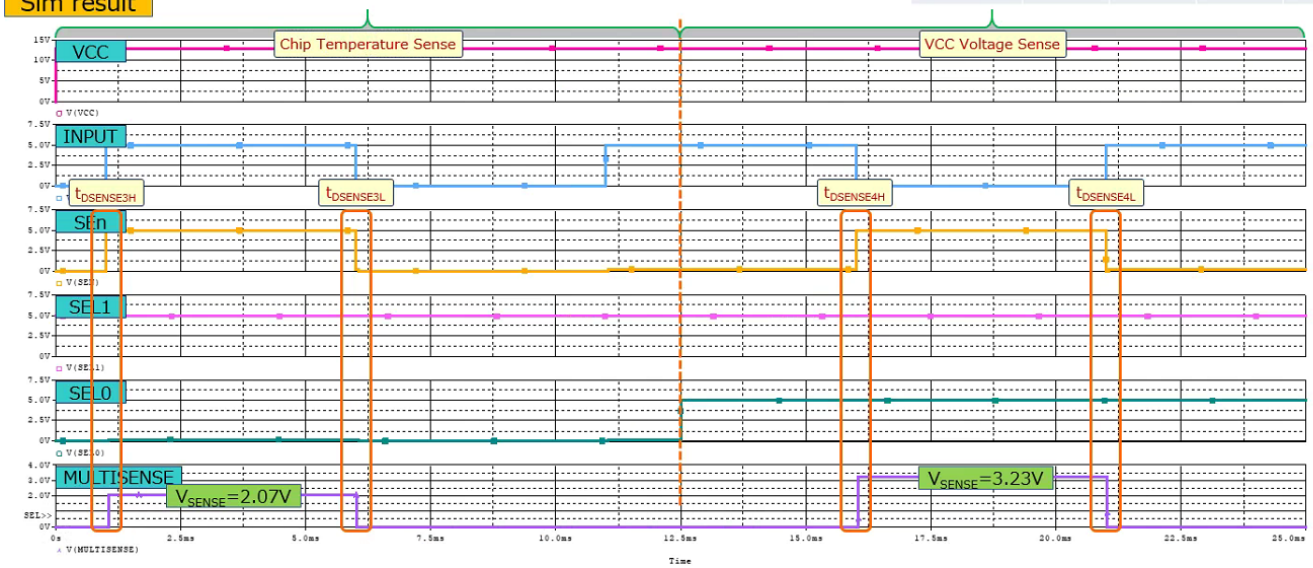


Multisense timings (chip temperature and VCC sense mode)

Simulation results are following.
Explanatory notes — : simulated

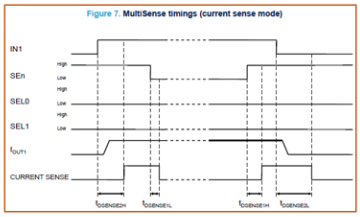
	$t_{DSENSE3H}$	$t_{DSENSE3L}$	$t_{DSENSE4H}$	$t_{DSENSE4L}$
Data sheet	60us	20us	60us	20us
Sim	55us	20us	55us	20us

Sim result

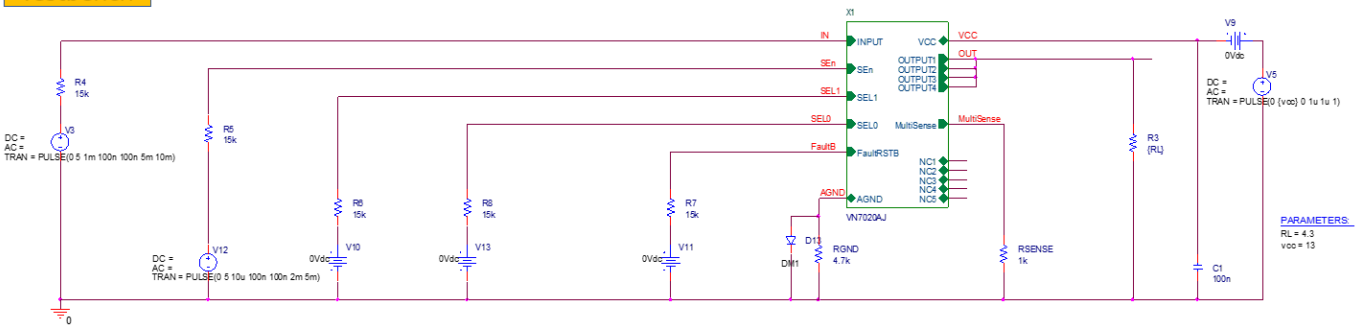


MultiSense timings (current sense mode)

Simulation results are following.
Explanatory notes — : simulated



Testbench

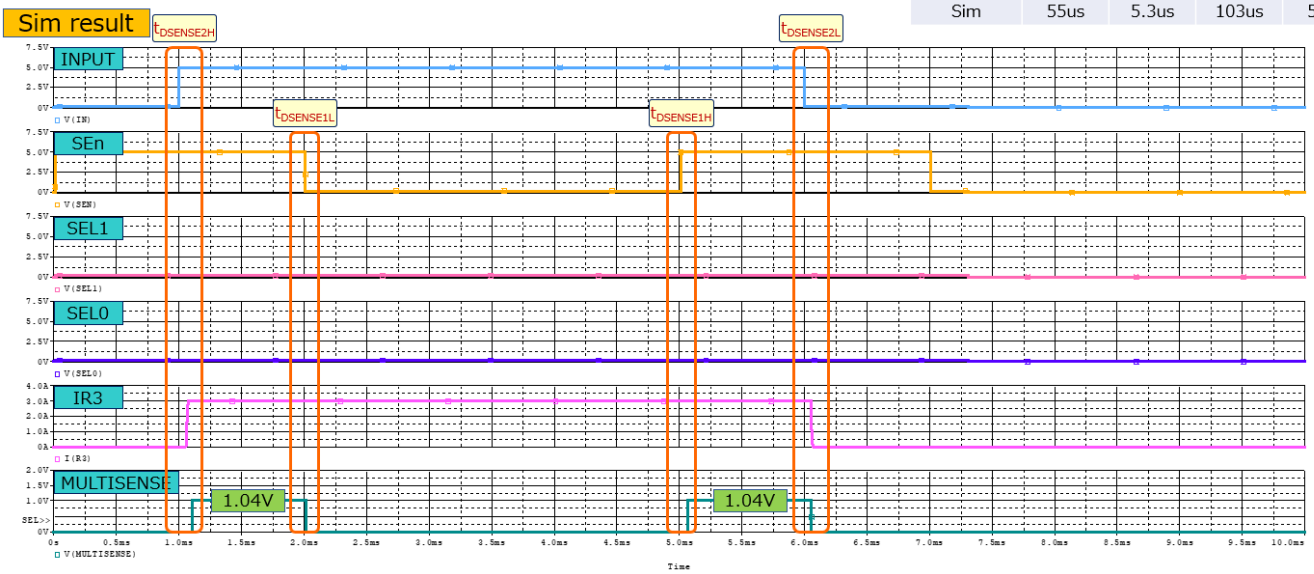


MultiSense timings (current sense mode)

Simulation results are following.
Explanatory notes — : simulated

	$t_{DSENSE1H}$	$t_{DSENSE1L}$	$t_{DSENSE2H}$	$t_{DSENSE2L}$
Data sheet	60us	5us	100us	50us
Sim	55us	5.3us	103us	54us

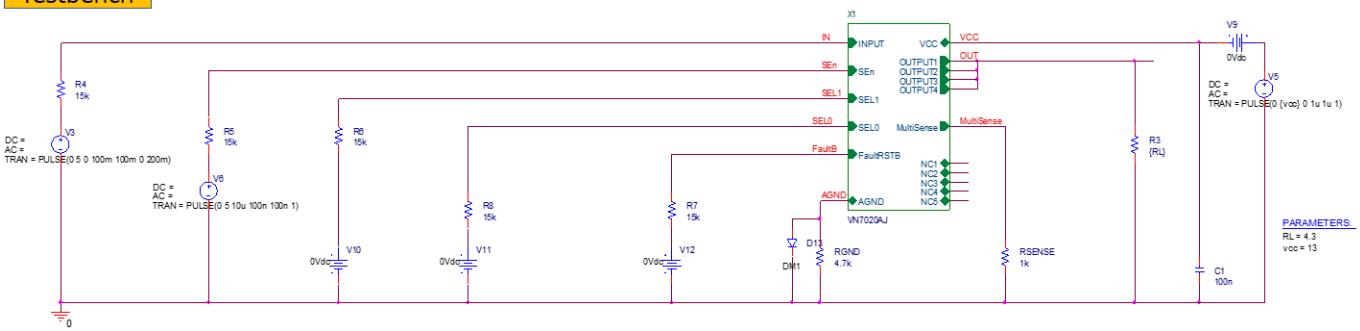
Sim result



Logic inputs (VIH=1.8V、VIL=1.35V)

Simulation results are following.
Explanatory notes　— : simulated

Testbench

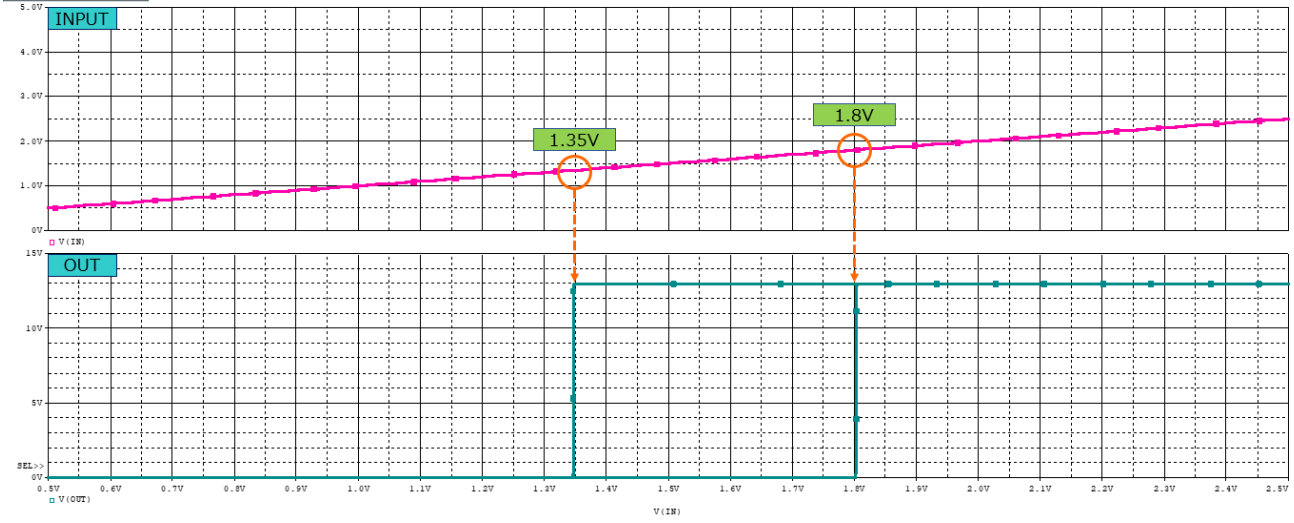


Logic inputs (VIH=1.8V、VIL=1.35V)

Simulation results are following.
Explanatory notes　— : simulated

	V_{IH}	V_{IL}
Data sheet	1.8V	1.35V
Sim	1.8V	1.35V

Sim result



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Modeling Design Technology

MoDeCH Inc.

Head Office
Location: 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan
Tel:+81-42-656-3360
E-Mail:model-on-support@modech.co.jp
URL:http://www.modech.com/en/