

# LTspice Model DCDC converter TEXAS INSTRUMENTS LM34966QPWPRQ1

# **Model Information**

Model A macro model

Call Name MDC\_LM34966QPWPRQ1\_LT

Pin Assign 1:BIAS 2:NC 3:VCC 4:GATE 5:PGND 6:AGND 7:CS

8:COMP 9:VDD 10:FB 11:SS 12:RT 13:PGOOD 14:EN\_UVLO\_SYNC 15:EP

File List Model Library MDC\_LM34966QPWPRQ1\_LT01.lib

Model Report MDC\_LM34966QPWPRQ1\_LT.pdf(this file)

Verified Simulator Version LTspice

Note

### References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version
 Product name
 Company name
 SEPTEMBER 2020
 LM34966QPWPRQ1
 TEXAS INSTRUMENTS

[Characteristics listed]

● Characteristics PWM Operation(Input=6V Output=24V IOUT=2A)

Overvoltage Protection Overload Protection

UVLO Shutdown and Clock synchronization UVLO Standby and Clock synchronization

### **Simulation Condition**

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C



## **Model Functions Table**

Function	Model
Dynamically programmable switching frequency from 100 kHz to 500 kHz	Ο
Optional clock synchronization	
Hiccup mode overload protection	Onote1
OVP protection	0
Adjustable soft start	0
PGOOD indicator	0

# Note 1

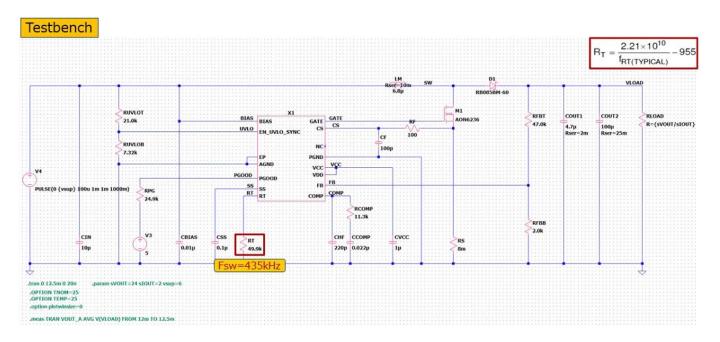
This model does not have a function to count the waiting time after transition to Hiccup mode.

An OFF latch function is installed as an alternative function.



PWM Operation(Input=6V Output=24V IOUT=2A)

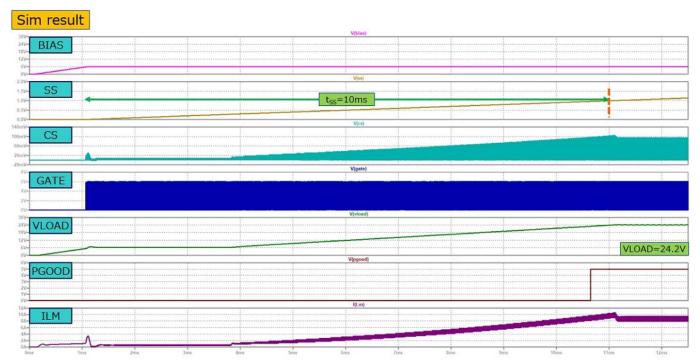
Simulation results are following. Explanatory notes — : simulated





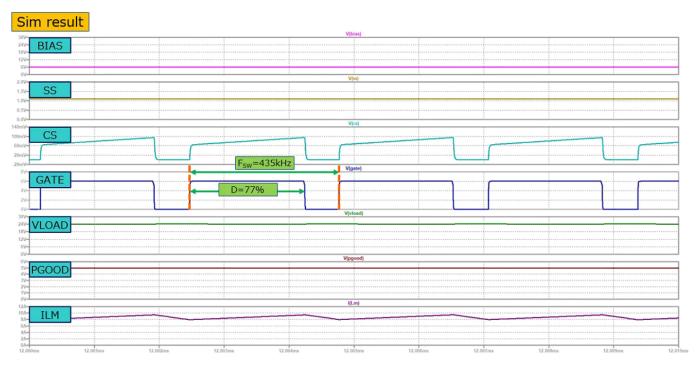
PWM Operation(Input=6V Output=24V IOUT=2A)

Simulation results are following. Explanatory notes — : simulated



PWM Operation(Input=6V Output=24V IOUT=2A)

Simulation results are following. Explanatory notes — : simulated

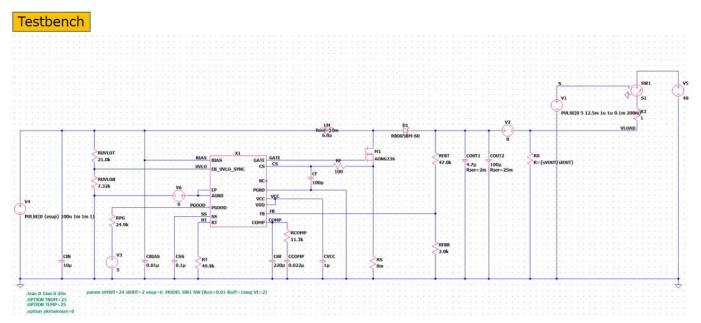




Overvoltage Protection

Simulation results are following.

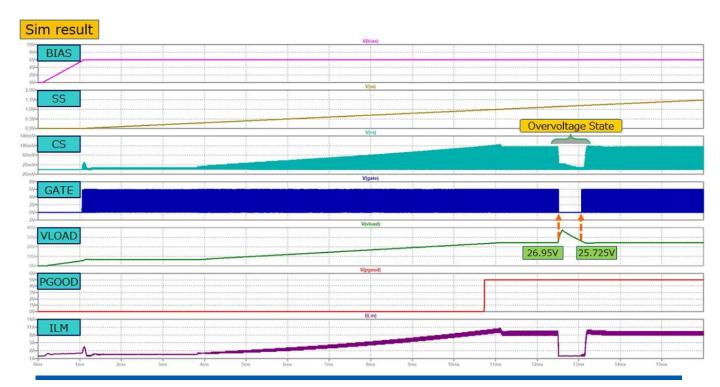
Explanatory notes — : simulated



Overvoltage Protection

Simulation results are following.

Explanatory notes — : simulated



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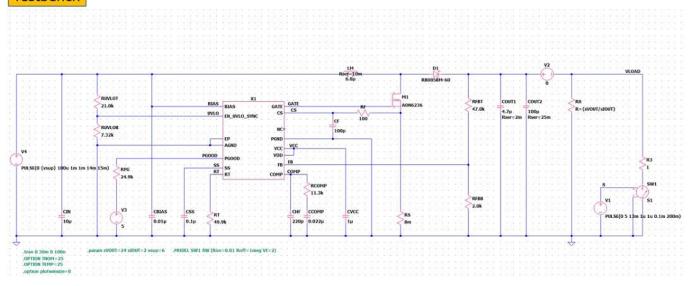


**Overload Protection** 

Simulation results are following.

Explanatory notes -: simulated

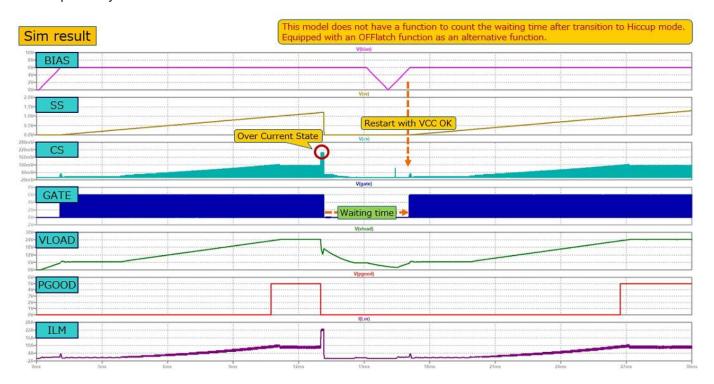
# Testbench





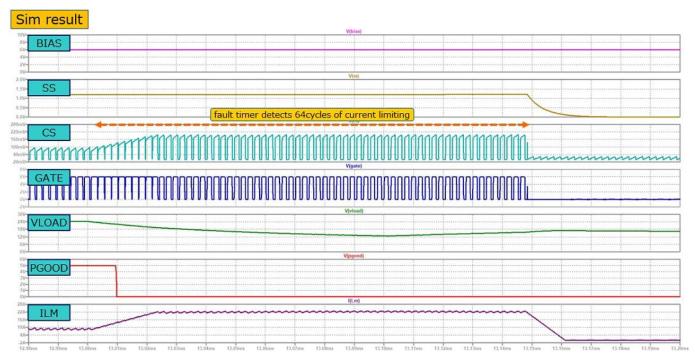
Overload Protection

Simulation results are following. Explanatory notes — : simulated



Overcurrent Protection(Input=12V Output=5.0V IOUT=2.1A⇒5.0A⇒2.1A)

Simulation results are following. Explanatory notes — : simulated

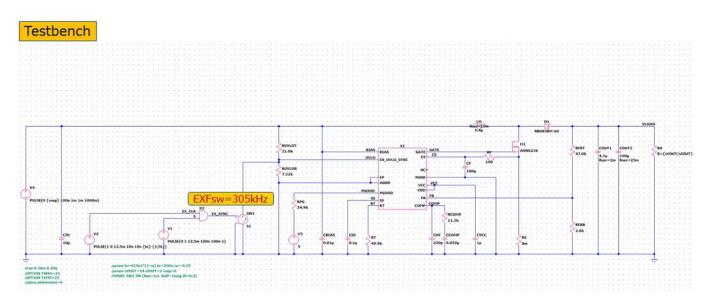




UVLO Shutdown and Clock synchronization

Simulation results are following.

Explanatory notes -: simulated

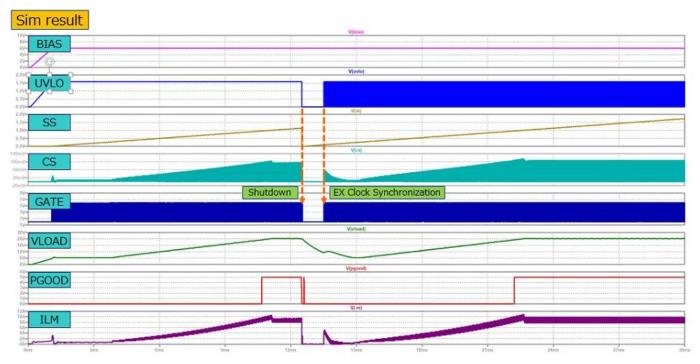




UVLO Shutdown and Clock synchronization

Simulation results are following.

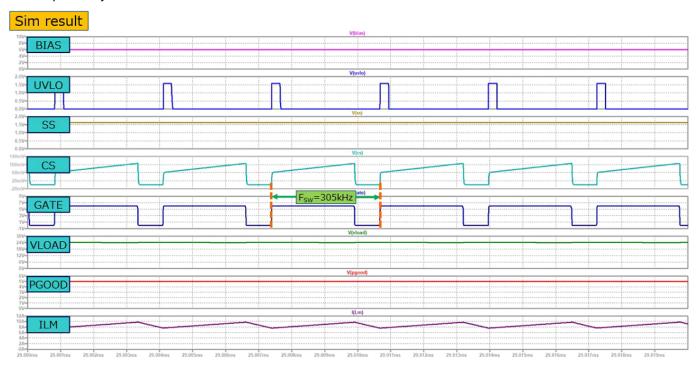
Explanatory notes — : simulated



UVLO Shutdown and Clock synchronization

Simulation results are following.

Explanatory notes — : simulated



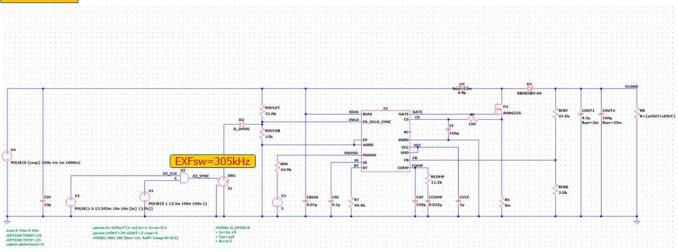


UVLO Standby and Clock synchronization

Simulation results are following.

Explanatory notes -: simulated

# Testbench

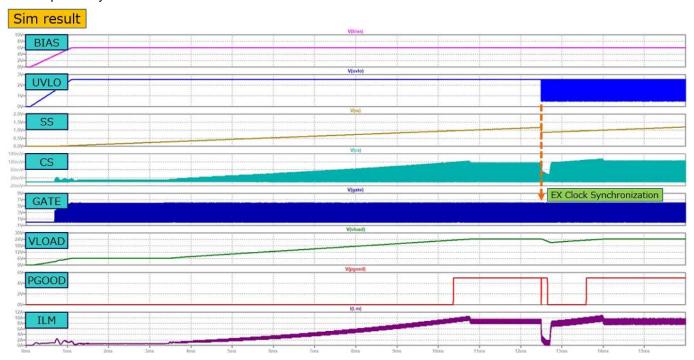




UVLO Standby and Clock synchronization

Simulation results are following.

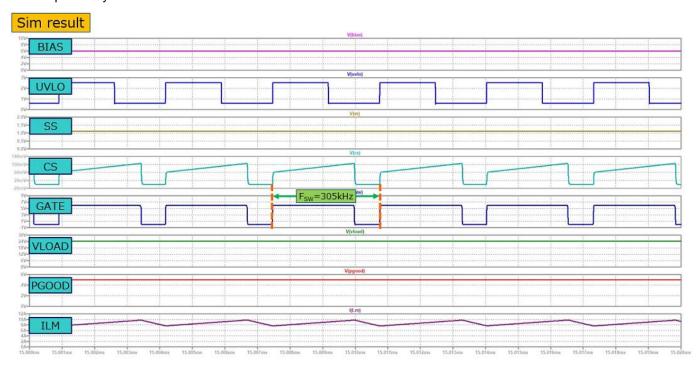
Explanatory notes -: simulated



UVLO Standby and Clock synchronization

Simulation results are following.

Explanatory notes — : simulated





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