

# LTspice Model

## LDO

### Torex Semiconductor

### XC6223T331MR-G

#### Model Information

**Model** A macro model  
**Call Name** MDC\_XC6223T331MR-G\_LT  
**Pin Assign** 1:VIN 2:VSS 3:CE 4:NC 5:VOUT  
**File List** Model Library MDC\_XC6223T331MR-G\_LT03.lib  
 Model Report MDC\_XC6223T331MR-G\_LT.pdf(this file)  
**Verified Simulator Version** LTspice XVII

#### Note

#### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version N/A
- Product name XC6223T331MR-G
- Company name Torex Semiconductor

[Characteristics listed]

- Characteristics VIN-VOUT,Limit Current,Dropout Voltage  
Line Regulation,Load Regulation,CE

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

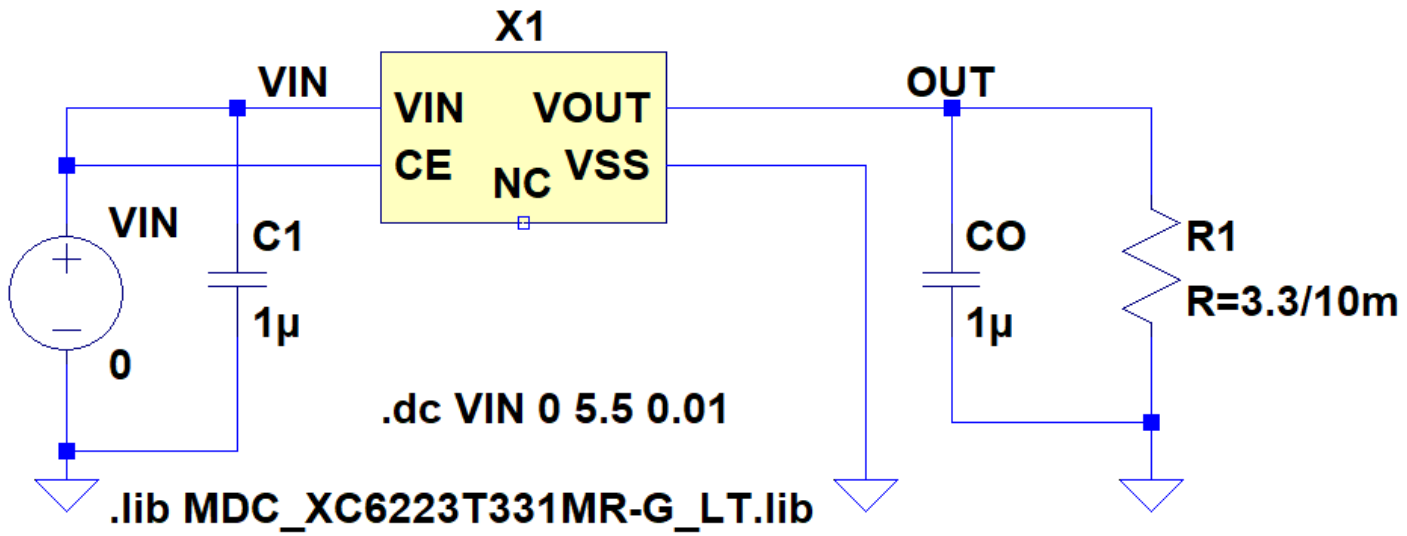
Item	Condition	Unit
Temperature	25	deg C

**Model Functions Table**

Functions	Implemented
VIN-VOUT	<input type="radio"/>
Limit Current	<input type="radio"/>
Dropout Voltage	<input type="radio"/>
Line Regulation	<input type="radio"/>
Load Regulation	<input type="radio"/>
CE	<input type="radio"/>

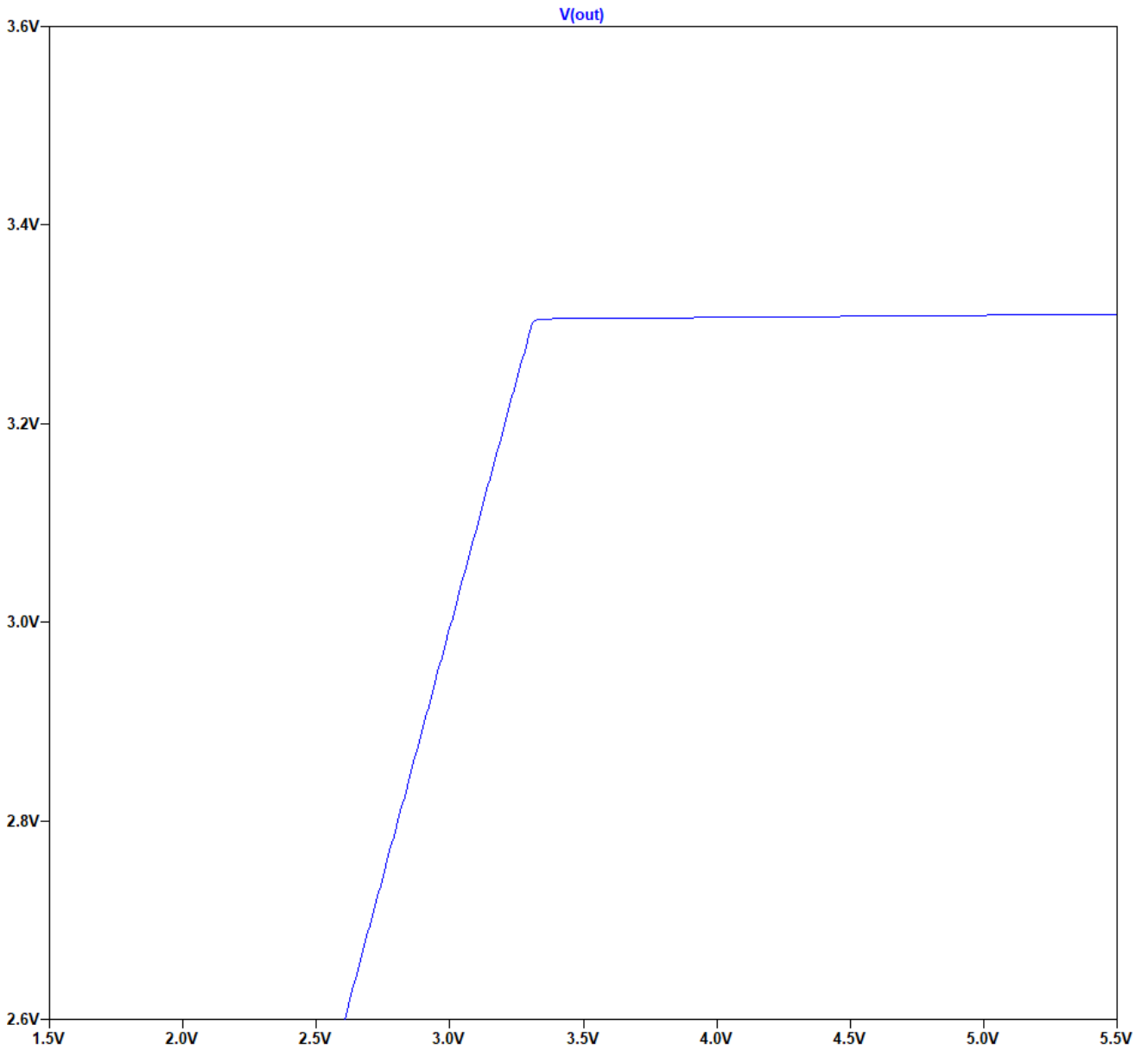
VIN-VOUT Testbench

Referred to Data Sheet



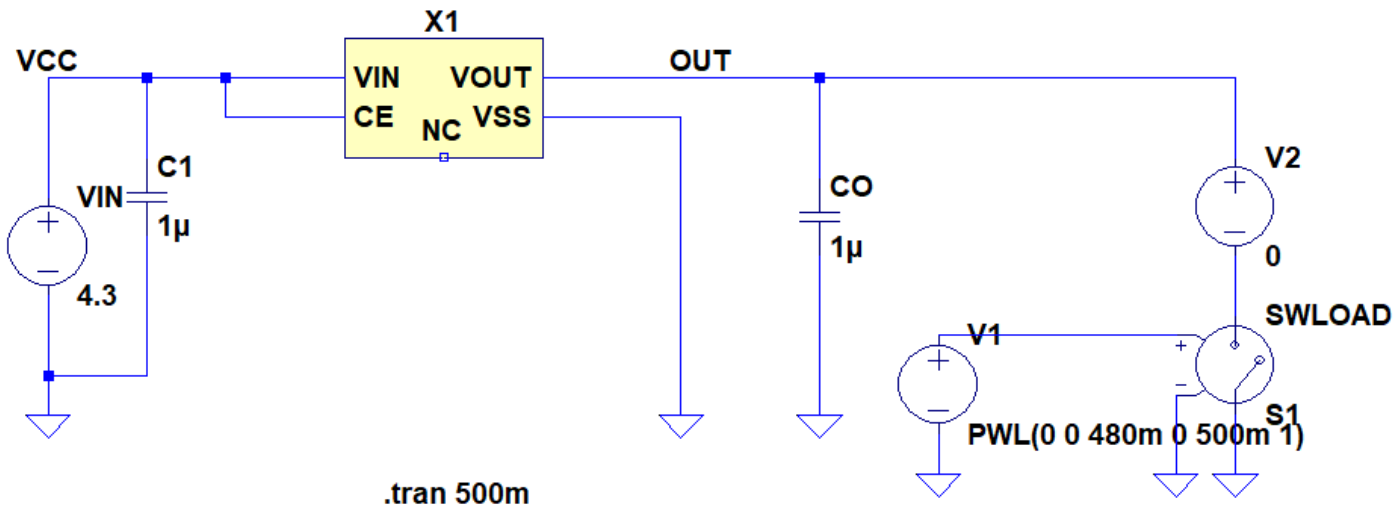
Simulation results are following.  
Explanatory notes — : simulated

VIN-VOUT



**Limit Current** Testbench

Referred to Data Sheet



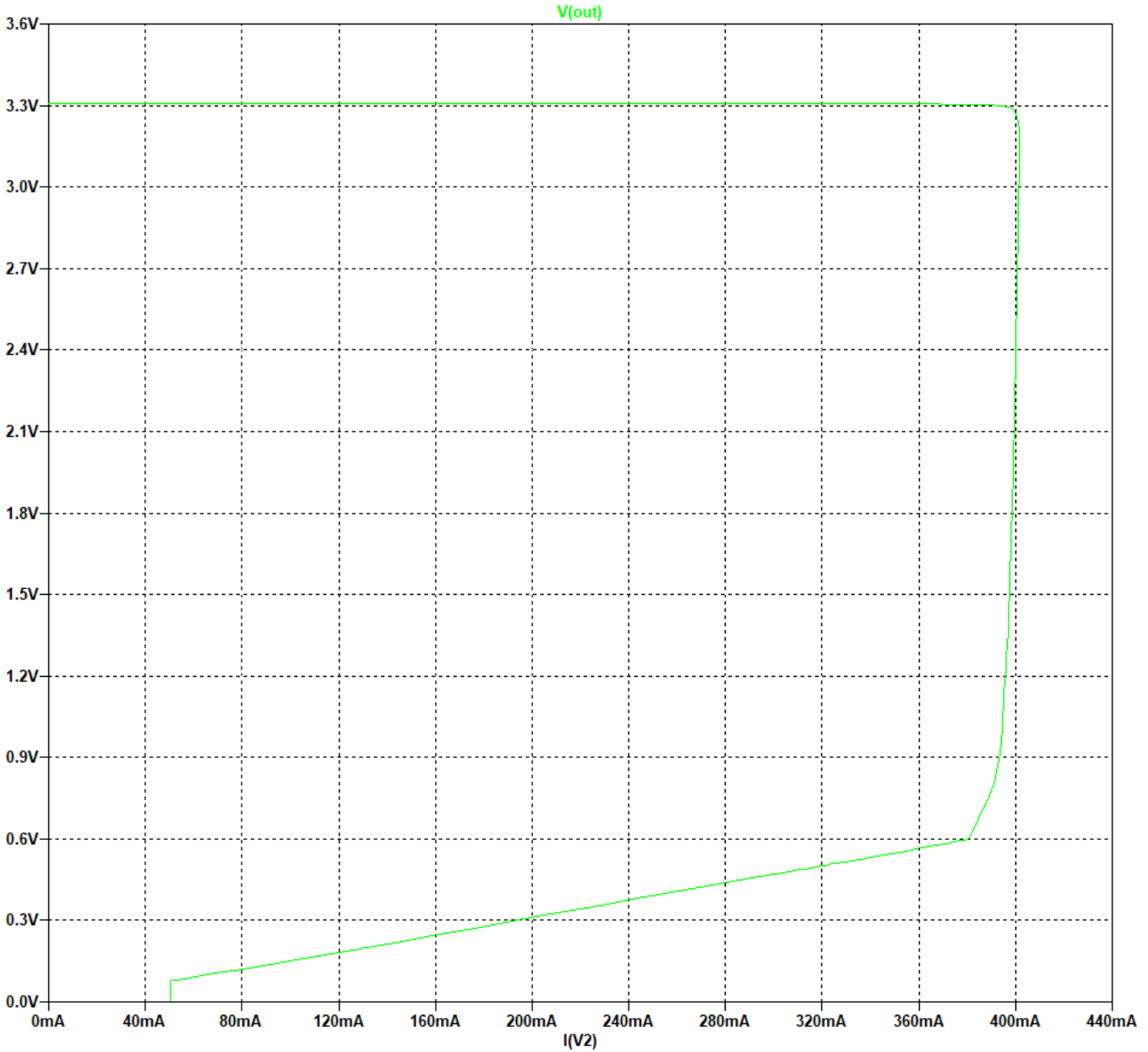
.tran 500m

.MODEL SWLOAD SW RON=1m ROFF=1Meg VON=1 VOFF=0

.lib MDC\_XC6223T331MR-G\_LT.lib

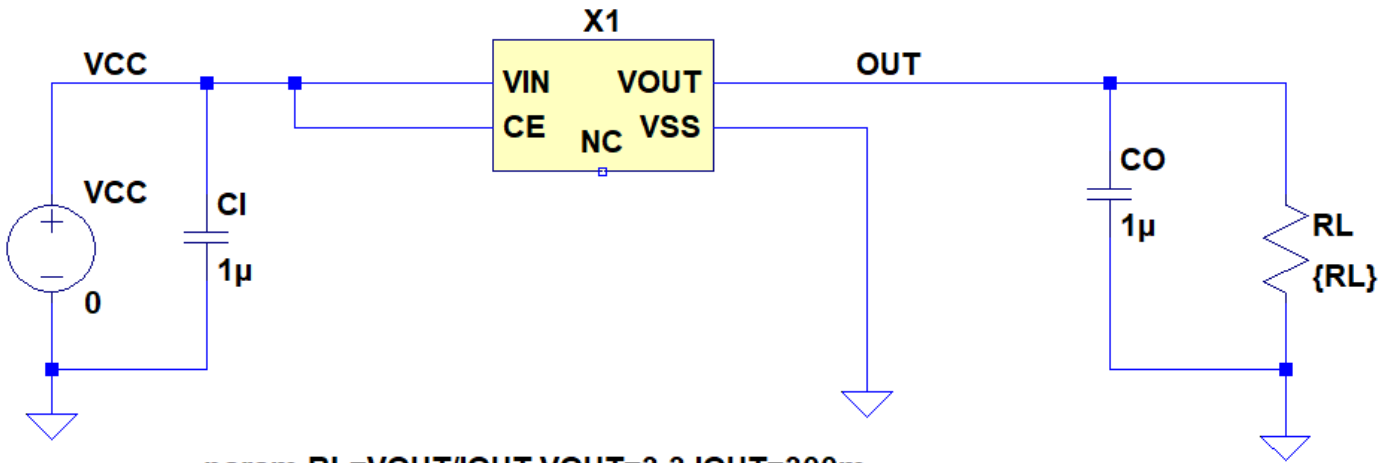
Simulation results are following.  
Explanatory notes — : simulated

**Limit Current**



**Dropout Voltage** Testbench

Referred to Data Sheet

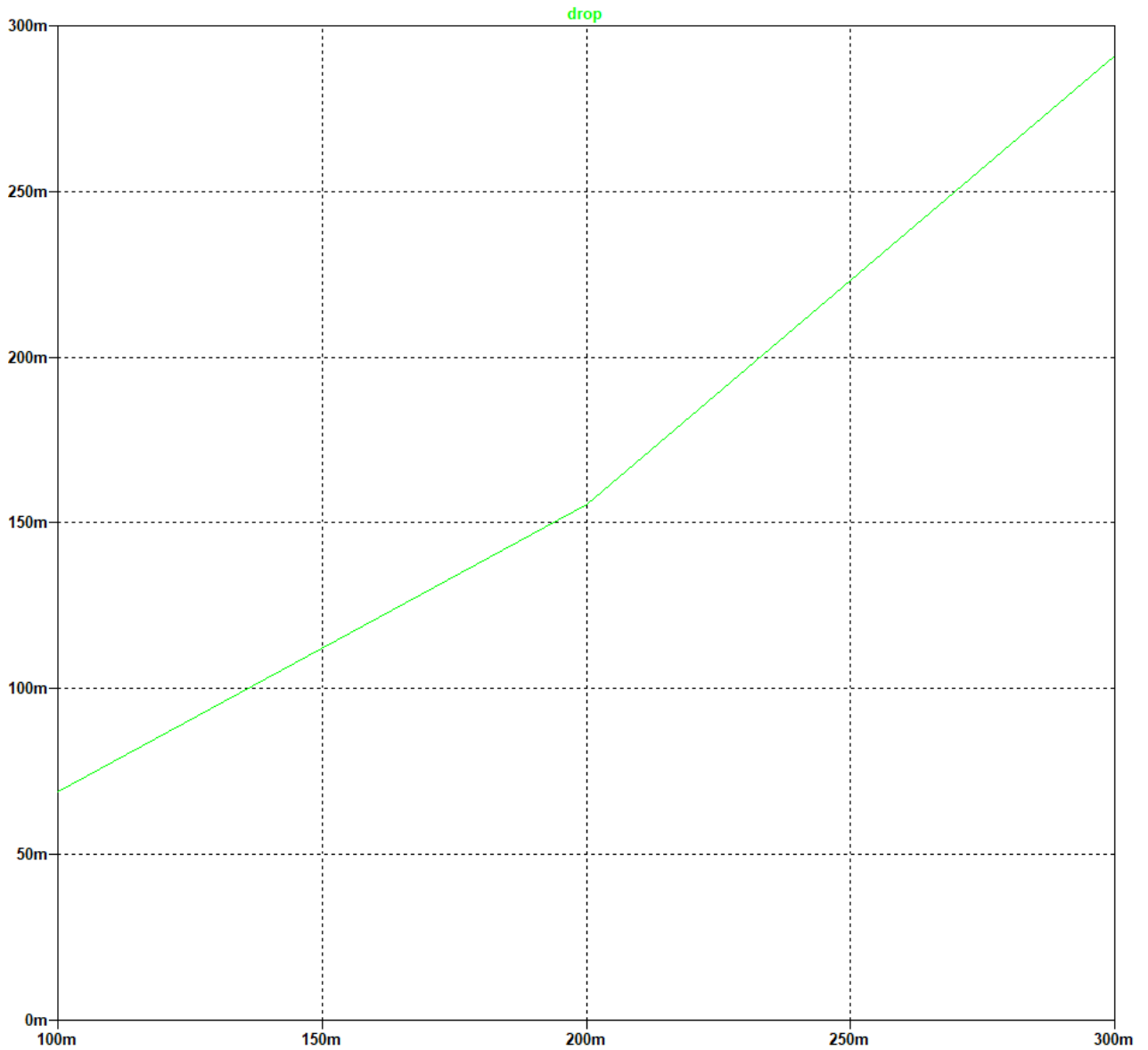


```

.param RL=VOUT/IOUT VOUT=3.3 IOOUT=300m
.dc VCC 0 5.5 0.01
.step param IOOUT 100m 300m 100m
.meas DC drop FIND V(VCC)-V(OUT) WHEN V(OUT)=3.2 RISE=1
.lib MDC_XC6223T331MR-G_LT.lib
    
```

Simulation results are following.  
Explanatory notes — : simulated

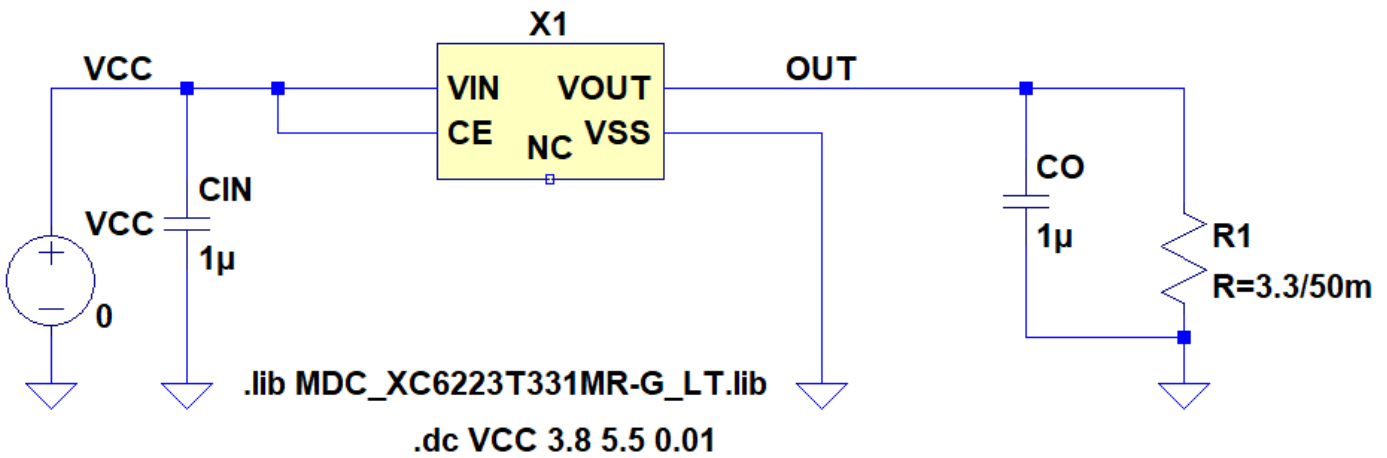
**Dropout Voltage**





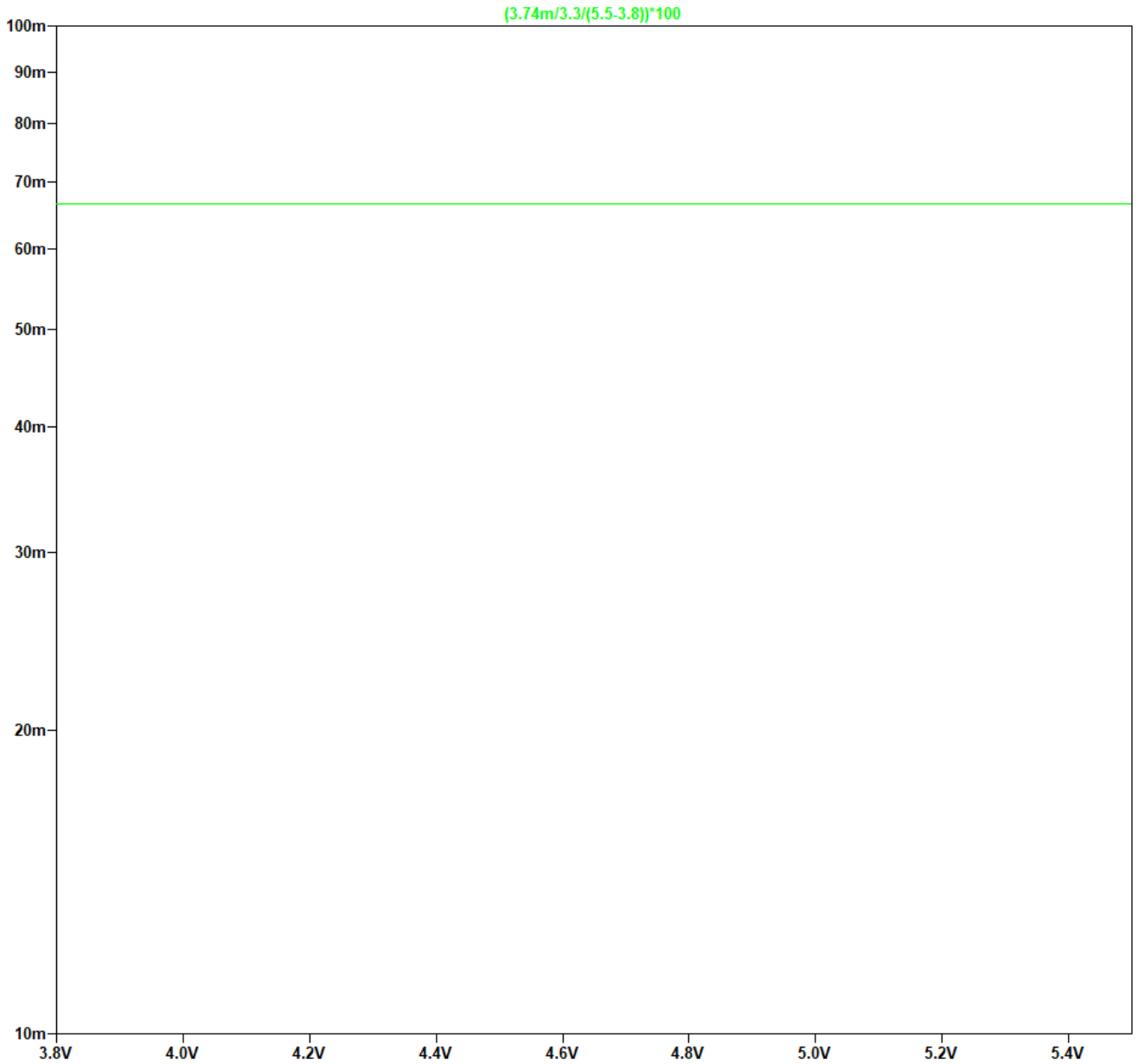
Line Regulation Testbench

Referred to Data Sheet



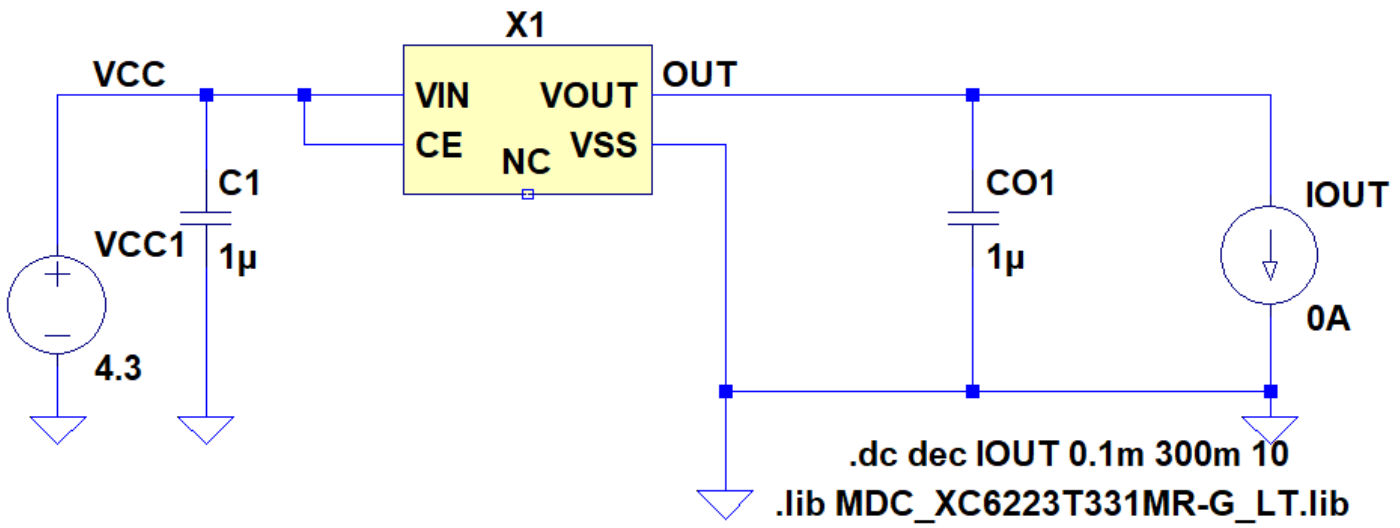
Simulation results are following.  
Explanatory notes — : simulated

**Line Regulation**



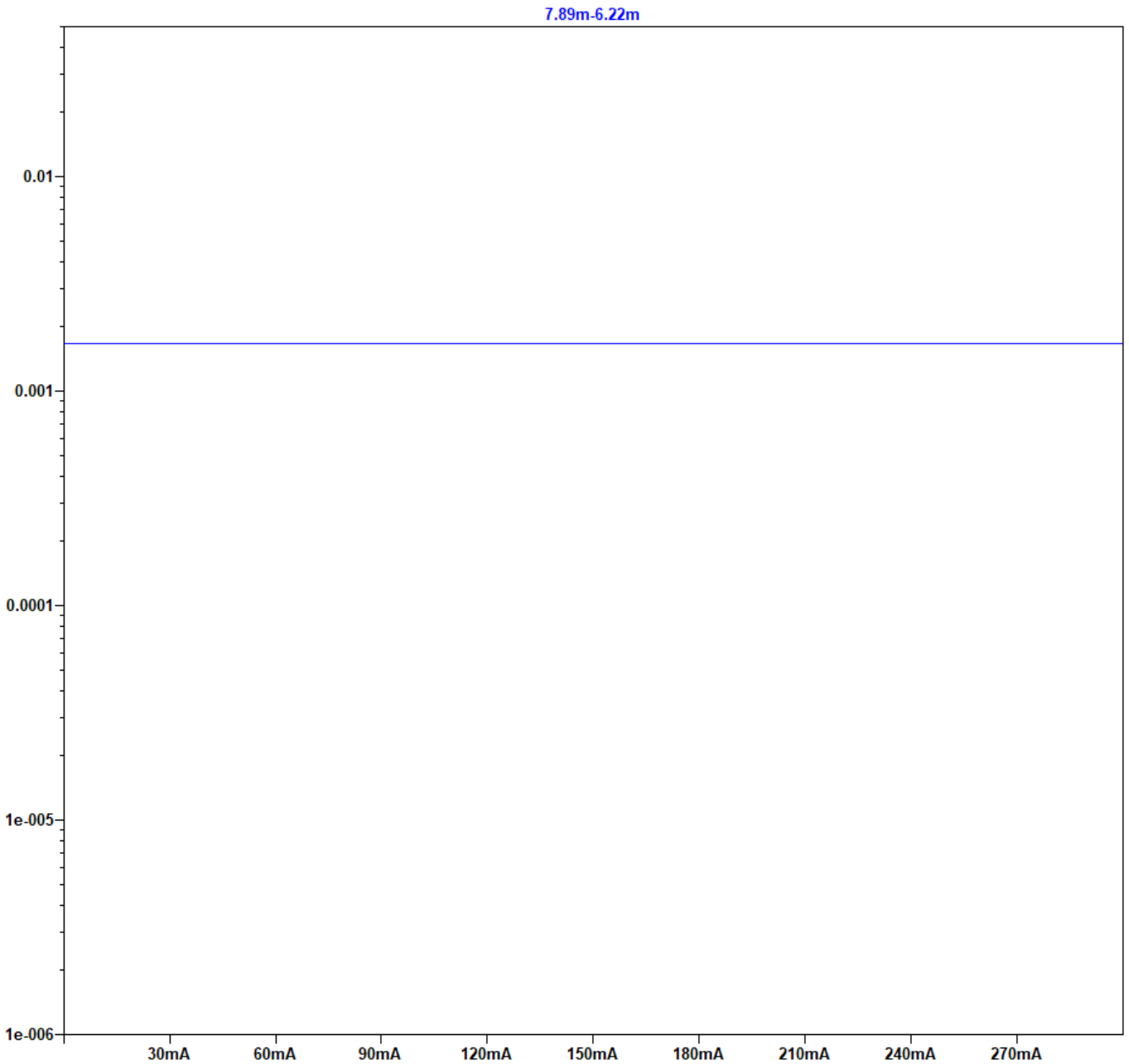
Load Regulation Testbench

Referred to Data Sheet



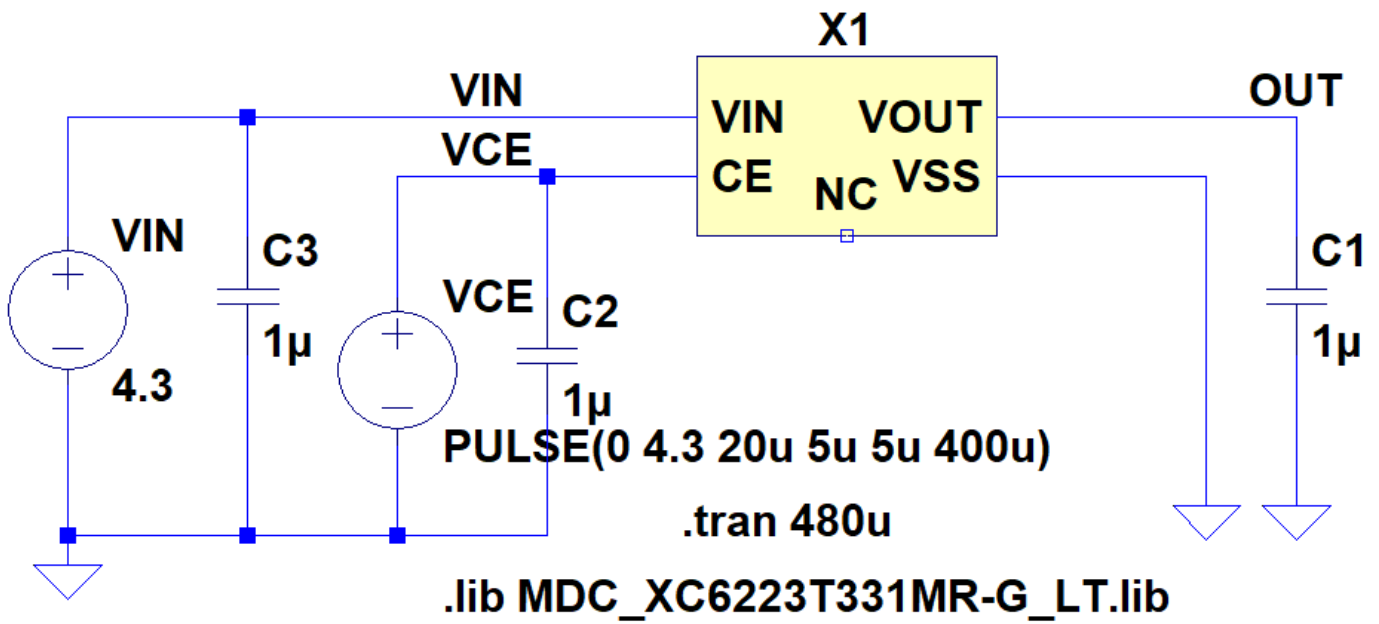
Simulation results are following.  
Explanatory notes — : simulated

**Load Regulation**



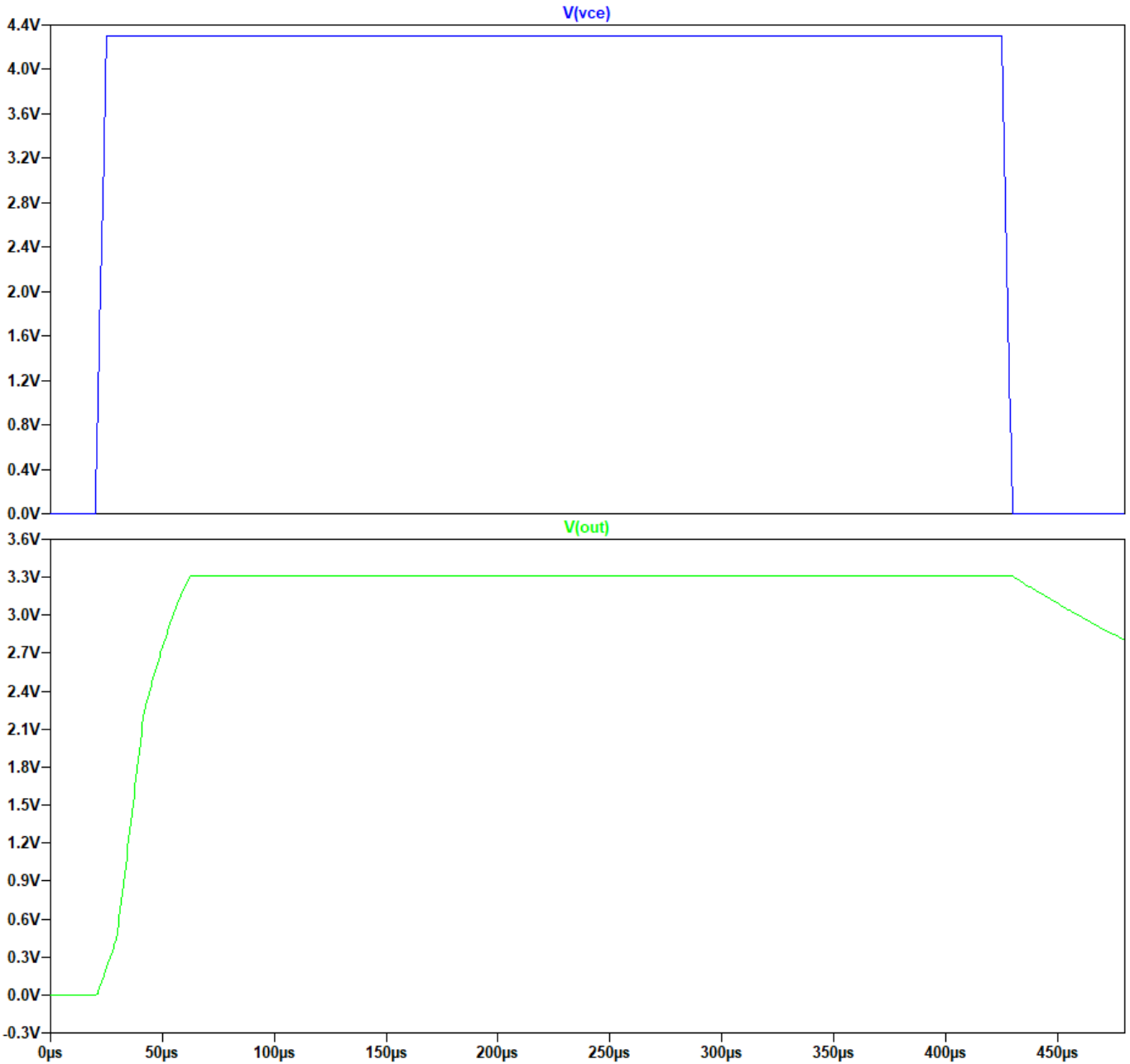
**CE Testbench**

Referred to Data Sheet



Simulation results are following.  
Explanatory notes — : simulated

**CE**



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