

LTspice Model Automotive ground sense comparator ROHM BA2903YFVM-M

Model Information

Model A macro model

Call Name MDC_BA2903YFVM-M_LT

Pin Assign 1:OUT1 2:-IN1 3:+IN1 4:VEE 5:+IN2 6:-IN2 7:OUT2 8:VCC

File List Model Library MDC_BA2903YFVM-M_LT.lib

Model Report MDC_BA2903YFVM-M_LT.pdf(this file)

Verified Simulator Version LTspice(x64) 24.0.9

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/VersionProduct name2013.9.13 Rev.002BA2903YFVM-M

Company name
ROHM

[Characteristics listed]

Characteristics Normal operation

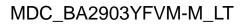
Circuit current
Input bias current
Input offset current
Input offset voltage
Output saturation voltage

Response time

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C





O: Implemented

×: Not Implemented
—: Not applicable

Model Functions Table

RANK=1

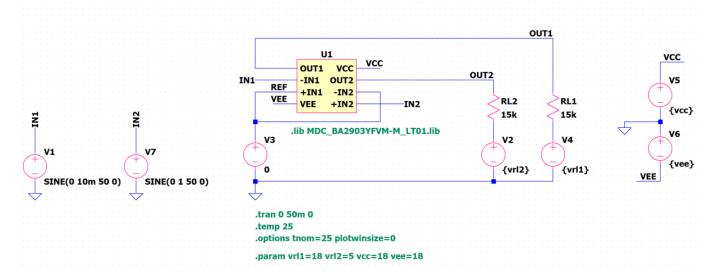
Functions	RANK	Implemented
Normal operation	1	0
Circuit current	1	0
Input bias current	1	0
Input offset current	1	0
Input offset voltage	1	0
Output saturation voltage	1	0
Response time	1	0



Normal operation

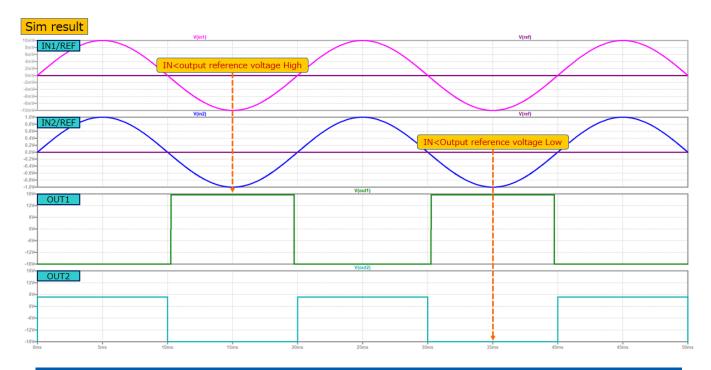
Simulation results are following. Explanatory notes — : simulated

Testbench



Normal operation

Simulation results are following. Explanatory notes — : simulated

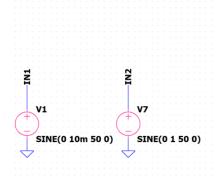


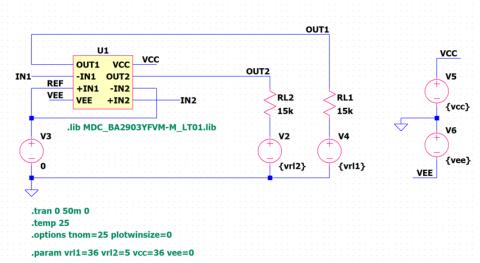


Normal operation

Simulation results are following. Explanatory notes — : simulated

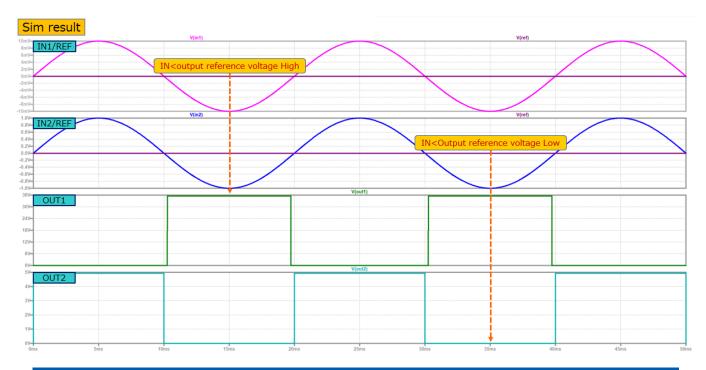
Testbench





Normal operation

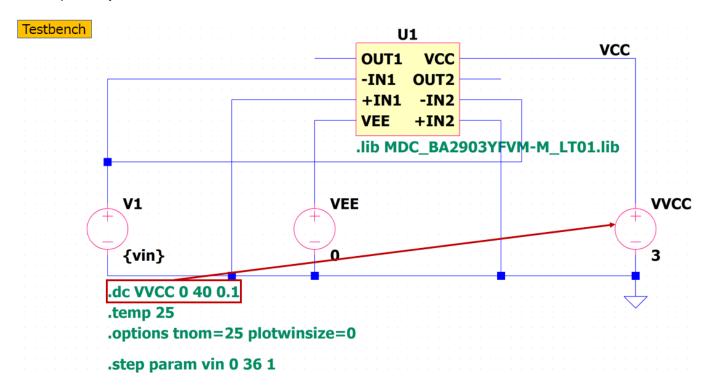
Simulation results are following. Explanatory notes — : simulated





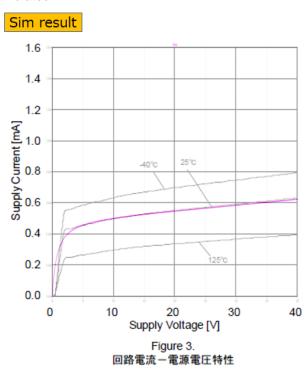
Circuit current

Simulation results are following. Explanatory notes — : simulated



Circuit current

Simulation results are following. Explanatory notes — : simulated





Input bias current

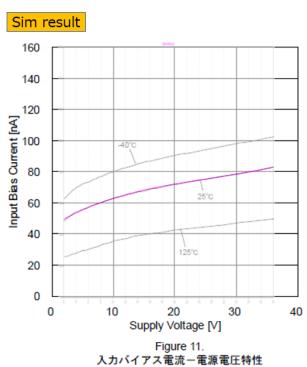
Simulation results are following. Explanatory notes — : simulated

Testbench U1 OUT1 VCC OUT1 VCC IN--IN1 OUT2 IN+ +IN1 -IN2 **VEE** +IN2 .lib MDC_BA2903YFVM-M_LT01.lib VIN-VIN+ **VEE VVCC** 0 3 0 .dc VVCC 2 36 0.1 .temp 25 .options tnom=25 plotwinsize=0

Input bias current

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Simulation results are following.





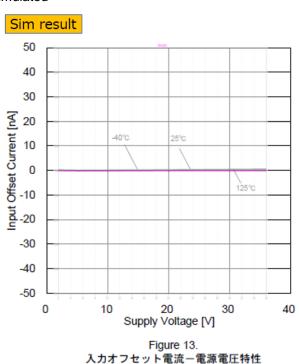
Input offset current

Simulation results are following. Explanatory notes — : simulated

Testbench U1 OUT1 VCC OUT1 VCC IN--IN1 OUT2 IN+ +IN1 -IN2 **VEE** +IN2 .lib MDC_BA2903YFVM-M_LT01.lib VIN-VEE **VVCC** VIN+ 0 3 0 .dc VVCC 2 36 0.1 .temp 25 .options tnom=25 plotwinsize=0

Input offset current

Simulation results are following.

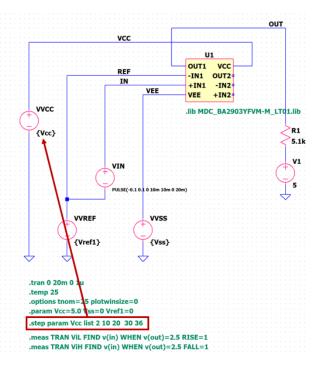




Input offset voltage

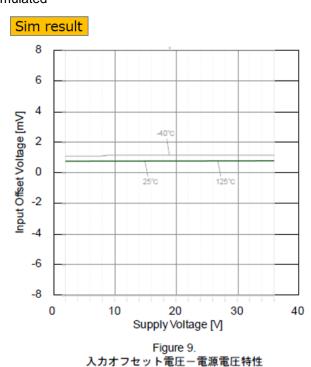
Simulation results are following. Explanatory notes — : simulated

Testbench



Input offset voltage
Simulation results are following.
Explanatory notes — : simulated

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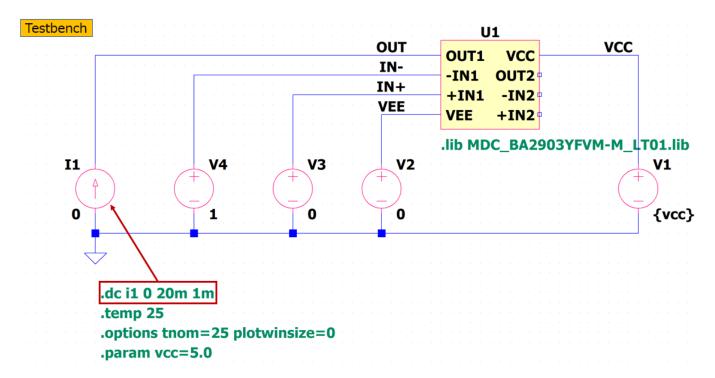




Output saturation voltage

Simulation results are following.

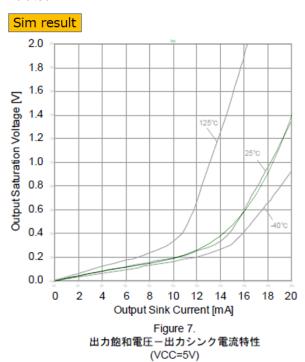
Explanatory notes — : simulated



Output saturation voltage

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Simulation results are following.

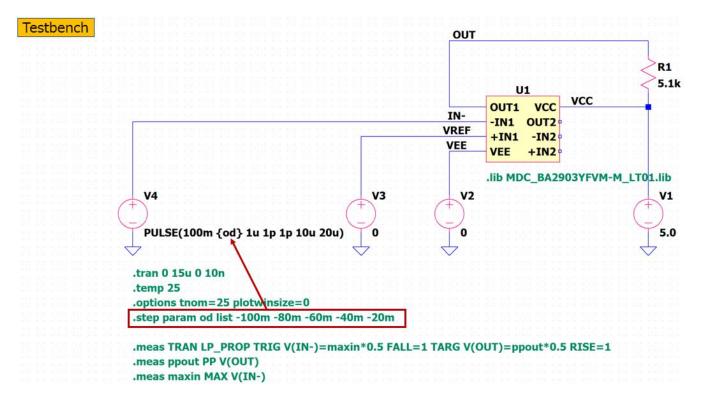


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Response time($L\rightarrow H$)

Simulation results are following. Explanatory notes — : simulated



Response time($L\rightarrow H$)

Simulation results are following.

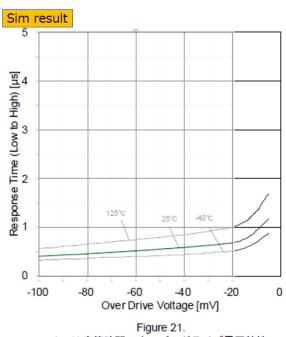
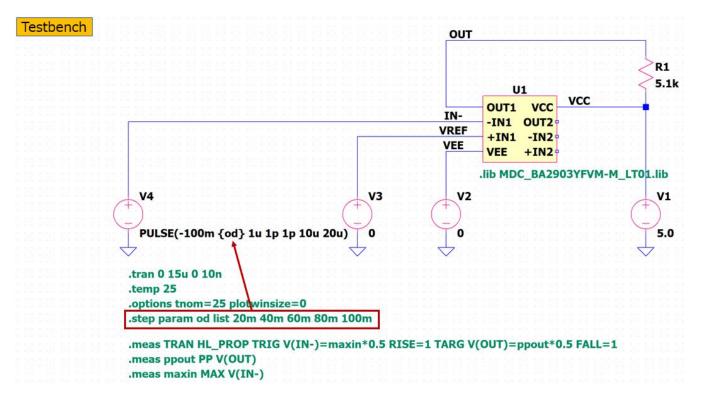


Figure 21. L→H 応答時間 ー オーバードライブ電圧特性 (VCC=5V, V_{RL}=5V, R_L=5.1kΩ)



Response time($H\rightarrow L$)

Simulation results are following. Explanatory notes — : simulated



Response time($H\rightarrow L$)

Simulation results are following.

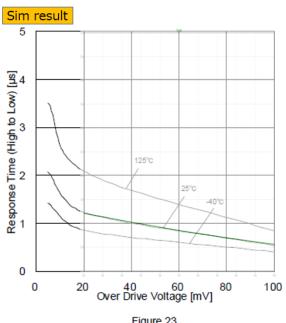


Figure 23. H→L 応答時間ーオーバードライブ電圧特性 (VCC=5V, V_{RL}=5V, R_L=5.1kΩ)



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