PSpice Model
NMOS+NMOS
TI
CSD87330Q3D

Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_CSD87330Q3D_PS	
Pin Assign	1:VIN 2:VIN 3:TG 4:TGR 5:BG 6:VSW 7:VSW 8 :VSW 9:PGND	
File List	Model Library	MDC_CSD87330Q3D_PS03.lib
	Model Report	MDC_CSD87330Q3D_PS.pdf (this file)
Verified Simulator Version		PSpice version 16.6
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version Rev. D
- ●Product name CSD87330Q3D
- ●Company name Texas Instruments Inc.
- ●Characteristics IdVds[Vgs],IdVgs[Temp],VgsQg[Vdd],Crss,Coss,Ciss,VthTemp[Id],Rds(on)Vgs[Temp],IsVsd[Temp],tdon,tdoff,tf,tr

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

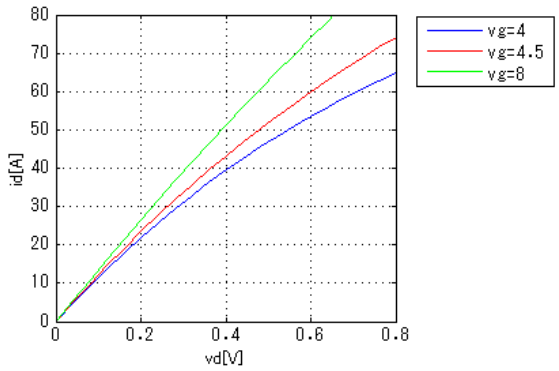
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	30	V
Gate-source voltage (DC)	0	to	8	V
Temperature	-55	to	150	deg C

Simulation results are following.
Explanatory notes — : simulated

Q1 (Control FET)

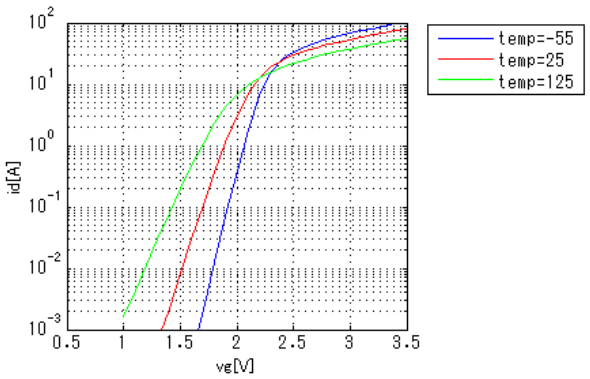
IdVds[Vgs]

Temp. = 25deg C



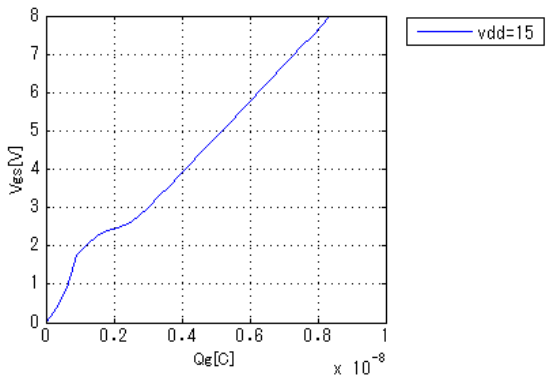
IdVgs[Temp]

Vds = 5V



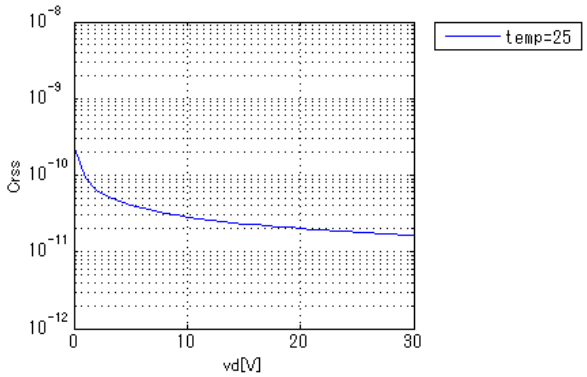
VgsQg[Vdd]

Id = 15A



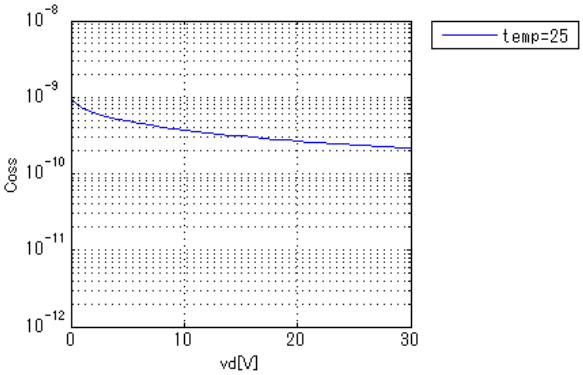
Crss

Freq. = 1MHz



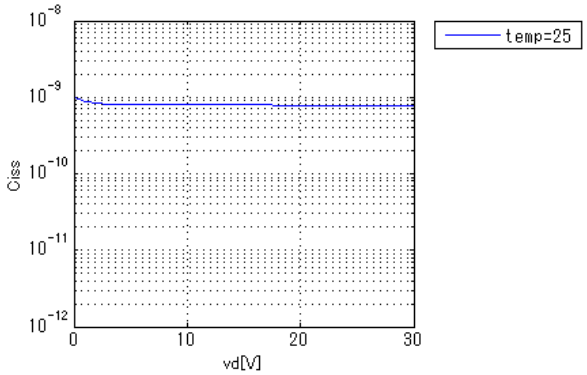
Coss

Freq. = 1MHz



Ciss

Freq. = 1MHz

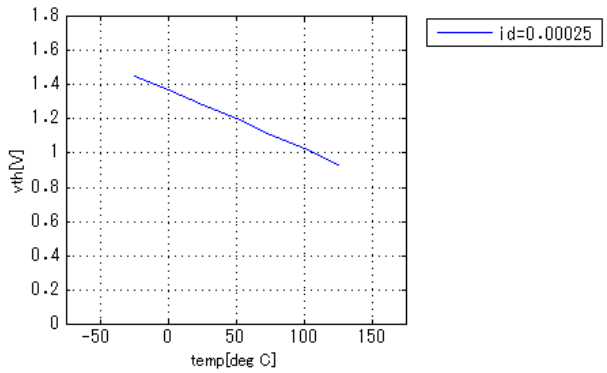


Simulation results are following.
Explanatory notes — : simulated

Q1 (Control FET)

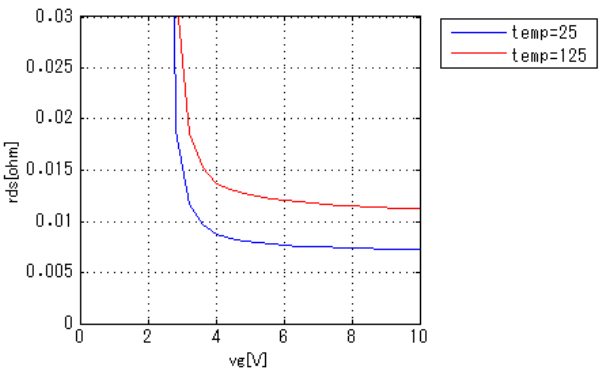
VthTemp[Id]

Vd = Vg

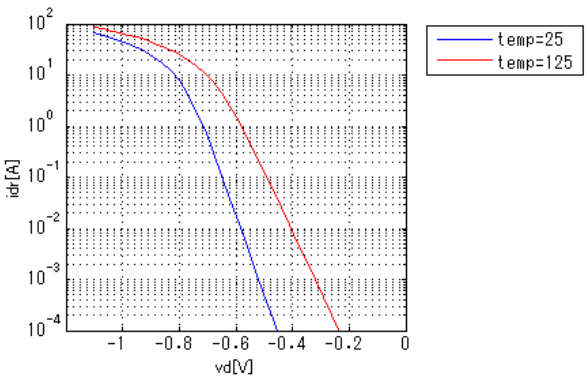


Rds(on)Vgs[Temp]

Id = 15A

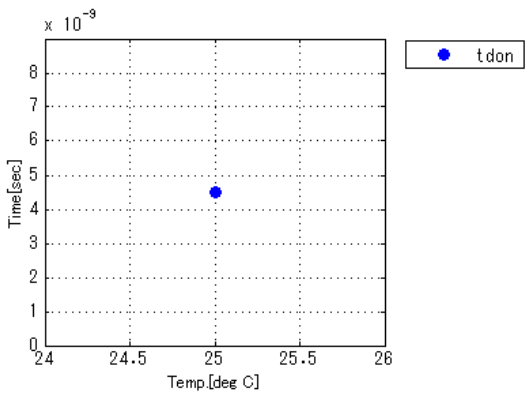


IsVsd[Temp]



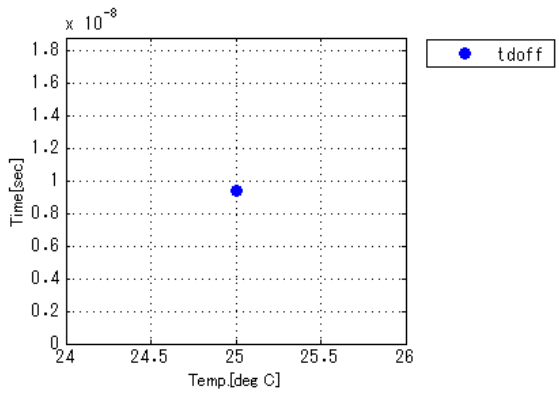
tdon

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm



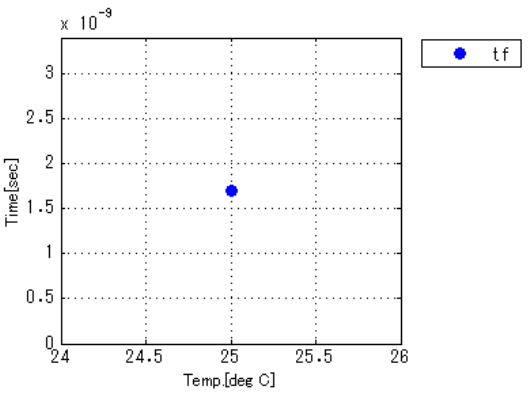
tdoff

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm



tf

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm

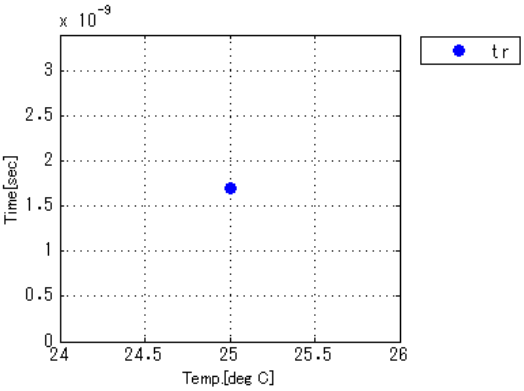


Simulation results are following.
Explanatory notes — : simulated

Q1 (Control FET)

tr

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm

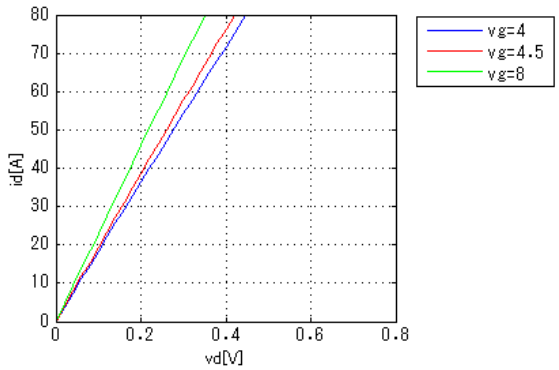


Simulation results are following.
Explanatory notes — : simulated

Q2 (Sync FET)

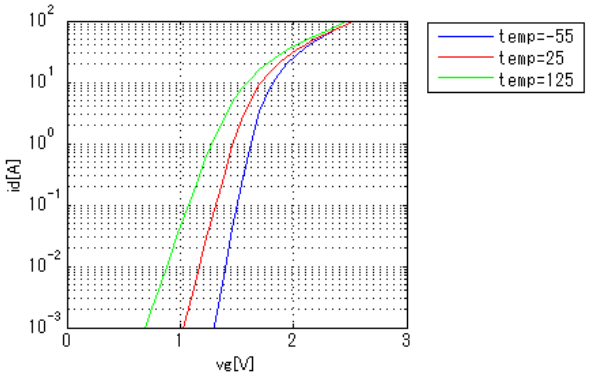
IdVds[Vgs]

Temp. = 25deg C



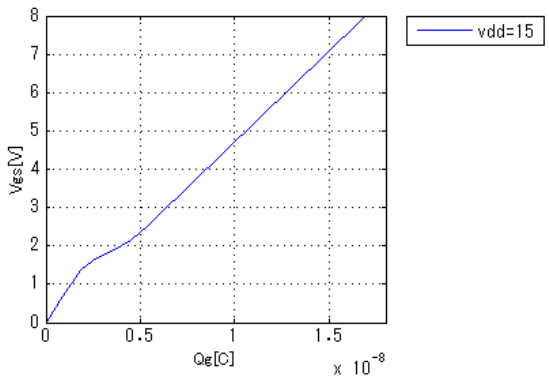
IdVgs[Temp]

Vds = 5V



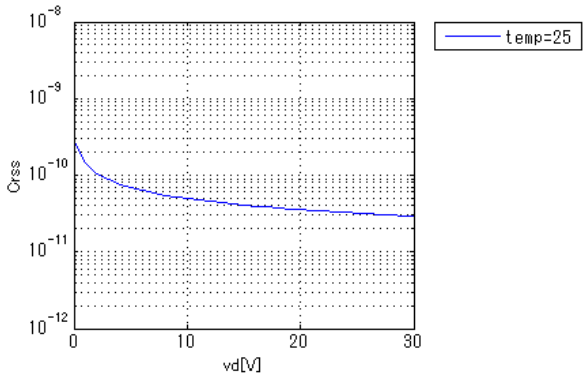
VgsQg[Vdd]

Id = 15A



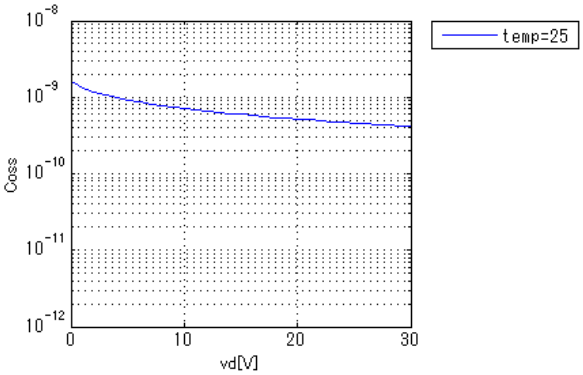
Crss

Freq. = 1MHz



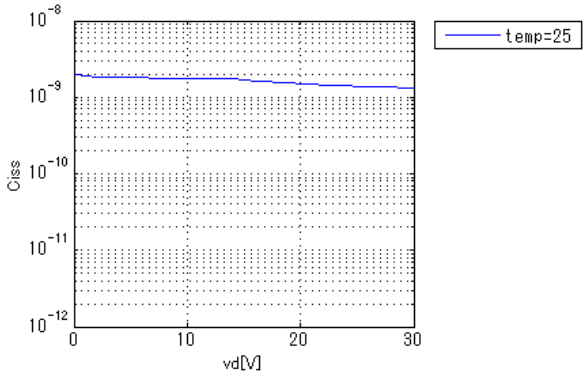
Coss

Freq. = 1MHz



Ciss

Freq. = 1MHz

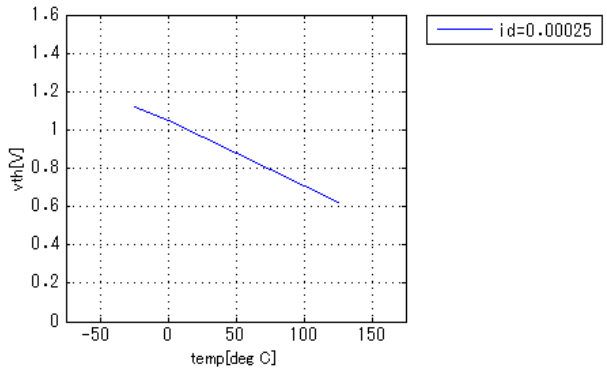


Simulation results are following.
Explanatory notes — : simulated

Q2 (Sync FET)

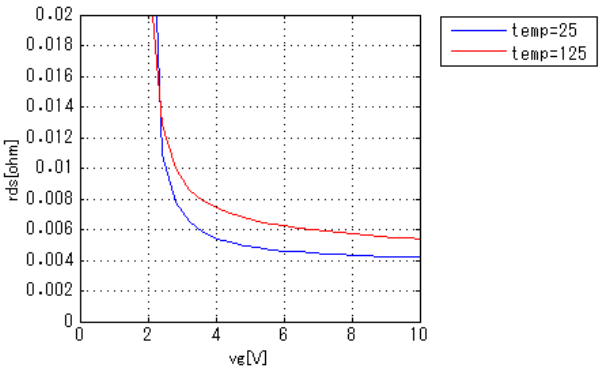
VthTemp[Id]

Vd = Vg

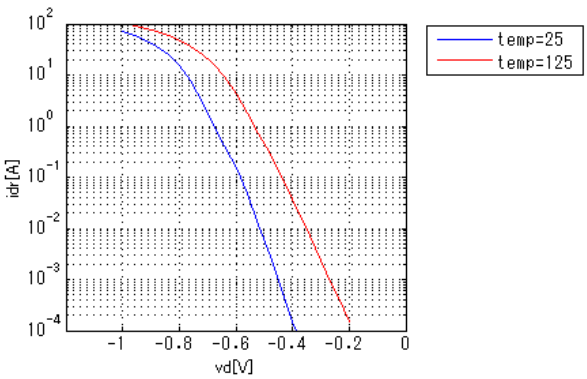


Rds(on)Vgs[Temp]

Id = 15A

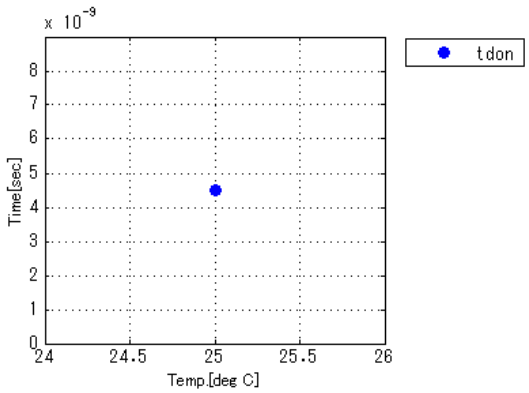


IsVsd[Temp]



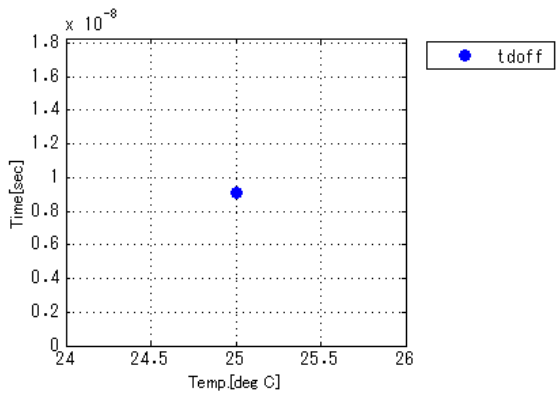
tdon

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm



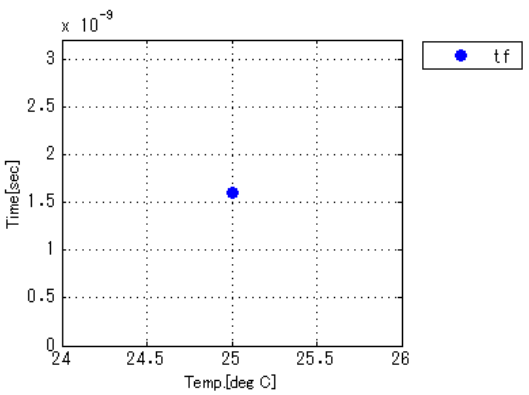
tdoff

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm



tf

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm

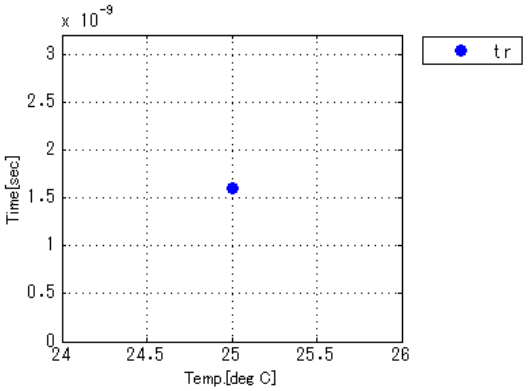


Simulation results are following.
Explanatory notes — : simulated

Q2 (Sync FET)

tr

Vdd = 15V, Id = 15A, +Vg = 4.5V, -Vg = 0V, Rg = 0.001ohm



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