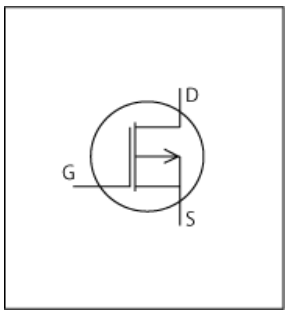
LTspice Model
PMOS
ON
ATP304



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_ATP304_LT	
Pin Assign	1:G 2:D 3:S 4:D(TAB)	
File List	Model Library	MDC_ATP304_LT02.lib
	Model Report	MDC_ATP304_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version: June, 2013
- ●Product name: ATP304
- ●Company name: ON Semiconductor.
- ●Characteristics: IdVds[Vgs],IdVgs[Temp],Rds(on)Vgs[Temp],Rds(on)Temp[Vgs],YfsId[Temp],IsVsd[Temp],CapacitanceVds[Cname],VgsQg[Vdd],SwitchingIdd[Tname]Rs,TrrIf[Ir],QrrIf[Ir],SwitchingWaveform,TrrWaveform

Simulation Range

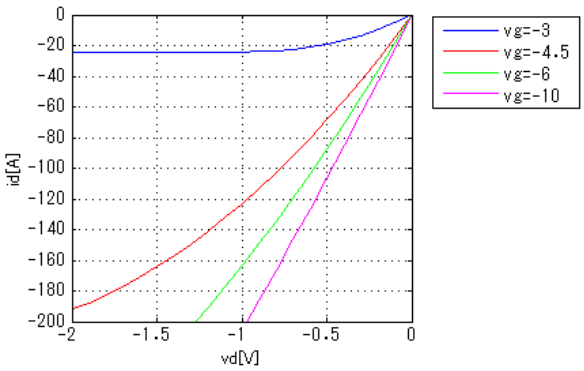
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-60	V
Gate-source voltage (DC)	20	to	-20	V
Temperature	-55	to	150	deg C

Simulation results are following.
Explanatory notes — : simulated

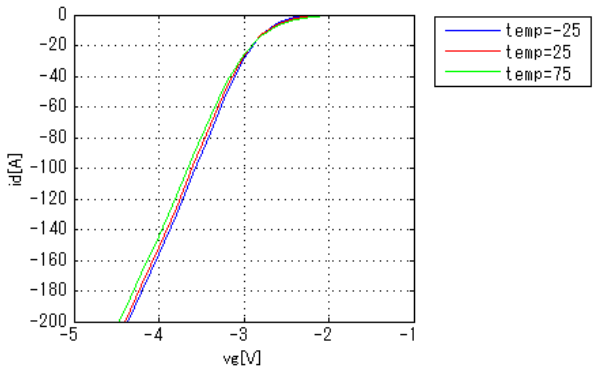
IdVds[Vgs]

Temp. = 25degC



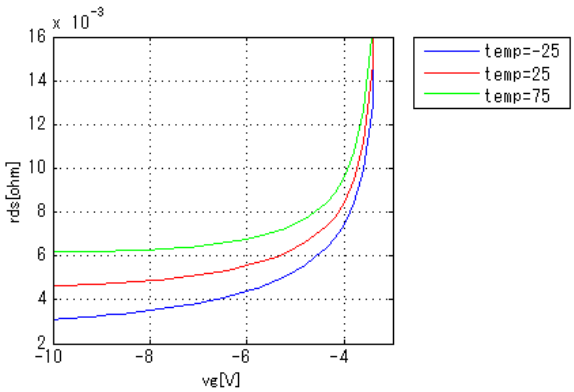
IdVgs[Temp]

Vds = -10V



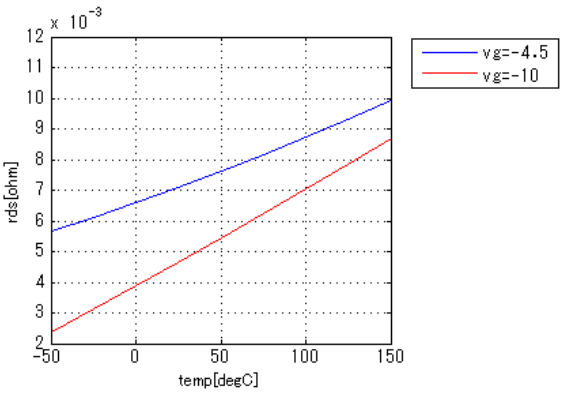
Rds(on)Vgs[Temp]

Id = -50A



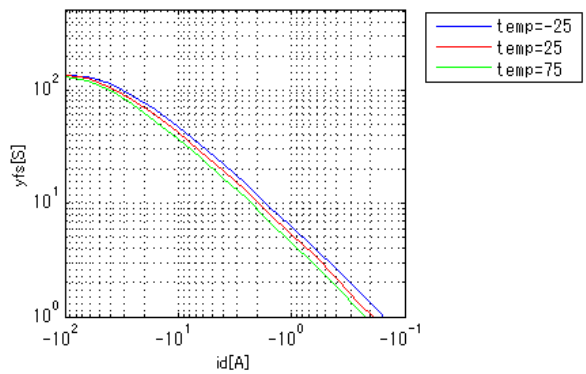
Rds(on)Temp[Vgs]

Id = -50A



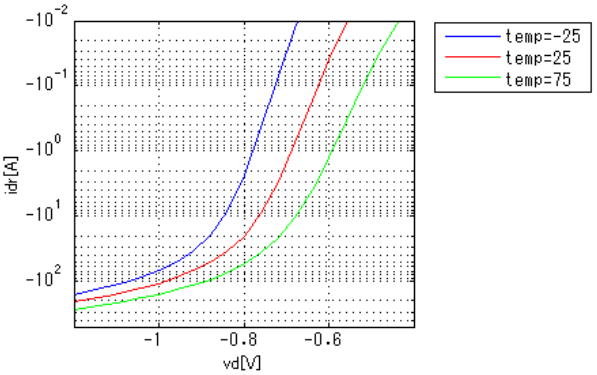
YfsId[Temp]

Vds = -10V



IsVsd[Temp]

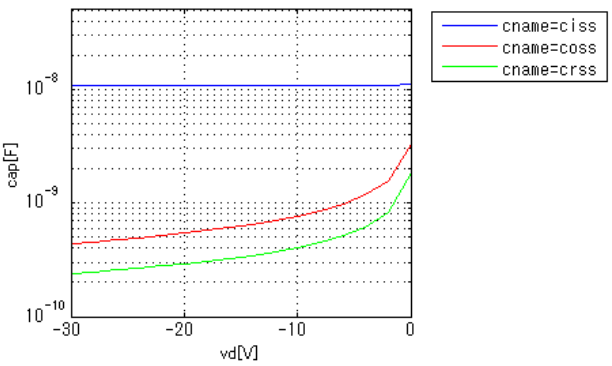
vg = 0V



Simulation results are following.
Explanatory notes — : simulated

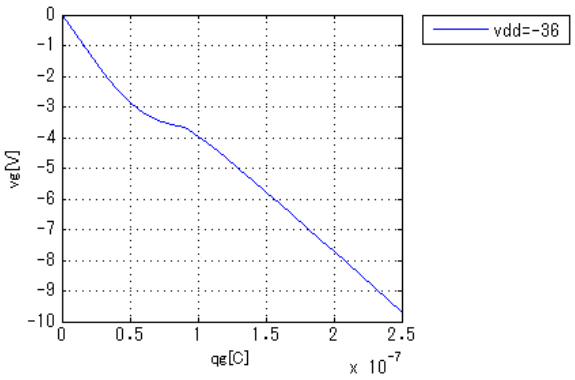
CapacitanceVds[Cname]

freq = 1000000Hz



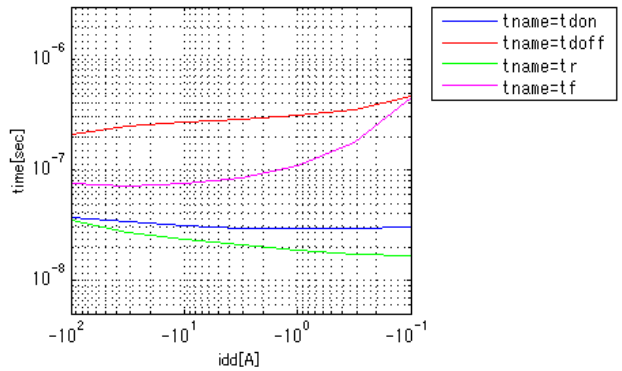
VgsQg[Vdd]

Id = -100A



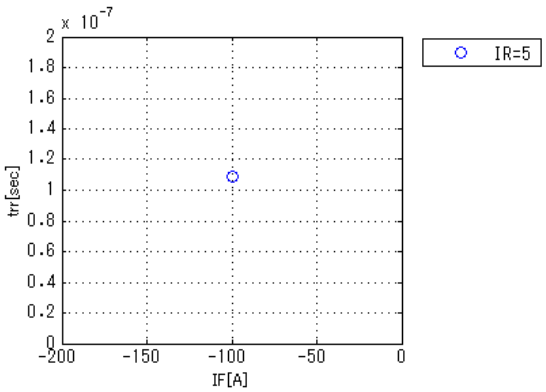
SwitchingIdd[Tname]Rs

vgg = -10V, vdd = -36V, RGS = 50ohm



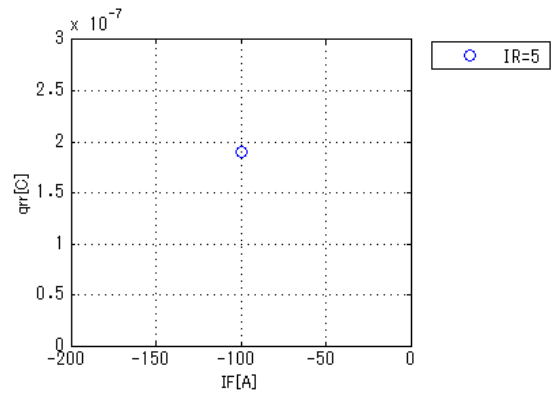
TrrIf[Ir]

vdd = -60V, didt = 100A/us, Temp = 25degC



QrrIf[Ir]

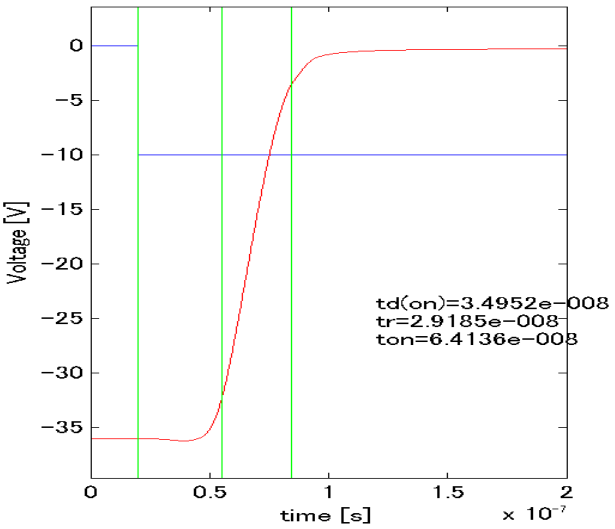
vdd = -60V, didt = 100A/us, Temp = 25degC

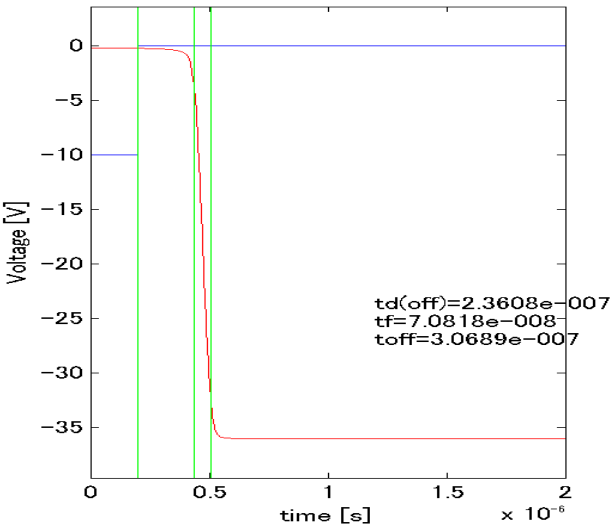


Simulation results are following.
Explanatory notes — : simulated

Switching Waveform (Blue : INPUT Red : OUTPUT)

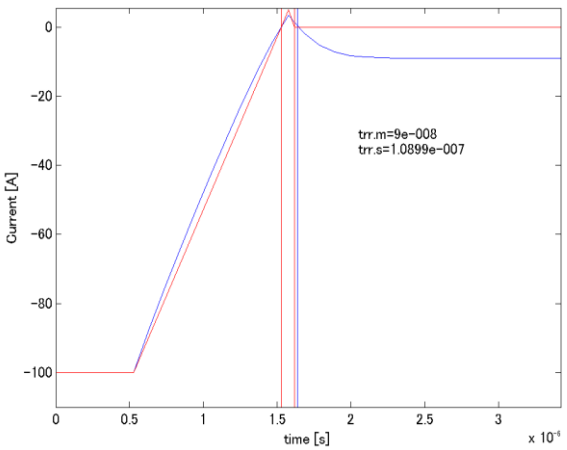
vgg = -10V, vdd = -36V, RGS = 50ohm, idd = -50A





Trr Waveform (Red : Datasheet Blue : Simulation)

vdd = -60V, didt = 100A/us, Temp = 25degC



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