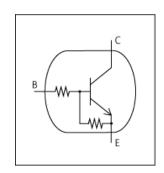


LTspice Model BRT (Bias Resistor Transistor) ROHM DTC123EKAT146



Model Information

Model A macro model based on Gummel-Poon model

Call Name MDC DTC123EKAT146 LT

Pin Assign 1:E 2:B 3:C

File List Model Library MDC_DTC123EKAT146_LT01.lib

Model Report MDC_DTC123EKAT146_LT.pdf (this file)

Verified Simulator Version

Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version
Product name
Company name
20151209 - Rev.003
DTC123EKAT146
ROHM Co., Ltd.

● Characteristics VionIc[Temp],IcVioff[Temp],IcVce[ib],hFEIc[Temp],Vce(sat)Ic

[Temp],fTle[Vce]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item		Range		
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
Collector currebt (DC)	0	to	100m	А
Temperature	-55	to	150	deg C
R1	2,200	to	2,200	ohm
R2	2,200	to	2,200	ohm



BRT

O: Implemented

×: Not Implemented

—: Not applicable

Model Functions Table RANK=1

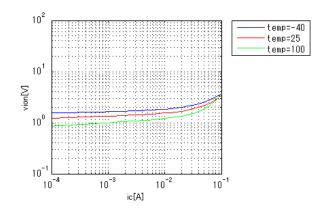
	10 (141)	
Functions	RANK	Implemented
VIN(on)-Iout(Temp)	1	0
Iout-VIN(off)(Temp)	1	0
Iout-Vo-Iin	1	0
DC_Current_Gain-Iout	1	0
VOUT(on)-Iout(Temp)	1	_
VOUT(sat)-Iout(Temp)	1	0
Capacitance	1	_
Transition Frequency	1	0
Switching(Typ.)	1	_



Simulation results are following. Explanatory notes — : simulated

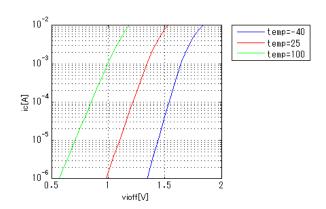
VionIc[Temp]

Vce = 0.3V



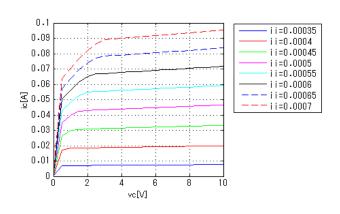
IcVioff[Temp]

Vce = 5V



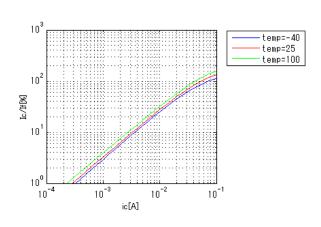
IcVce[ib]

Temp. = 25degC



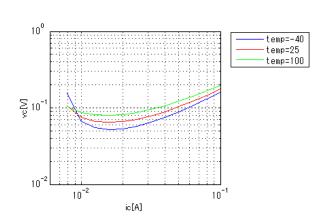
hFElc[Temp]

Vce = 5V

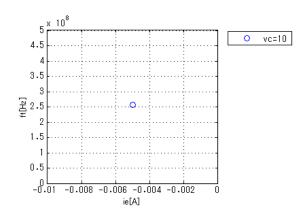


Vce(sat)lc[Temp]

IC/IB = 20



fTle[Vce]





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