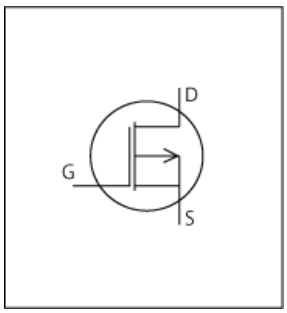
LTspice Model
PMOS
ON
ATP114-TL-H



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_ATP114-TL-H_LT	
Pin Assign	1:D 2:G 3:S	
File List	Model Library	MDC_ATP114-TL-H_LT01.lib
	Model Report	MDC_ATP114-TL-H_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version None
- ●Product name ATP114-TL-H
- ●Company name ON Semiconductor.
- ●Characteristics IdVds[Vgs],IdVgs[Temp],Rds(on)Vgs[Id],IsVsd[Temp],Crss,Coss,Ciss,VgsQg[Vdd],Rds(on)Temp[Id],tdon,tdoff,tf,tr

Simulation Range

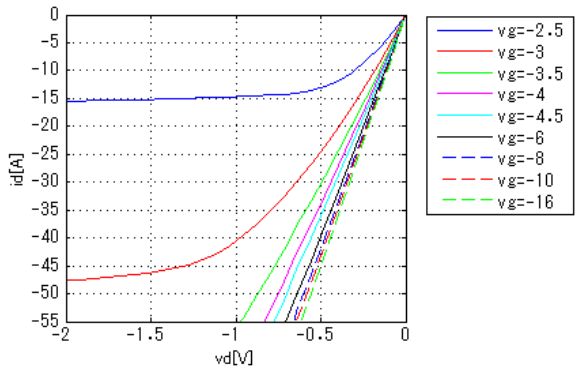
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-60	V
Gate-source voltage (DC)	0	to	-20	V
Temperature	-55	to	150	deg C

Simulation results are following.
Explanatory notes — : simulated

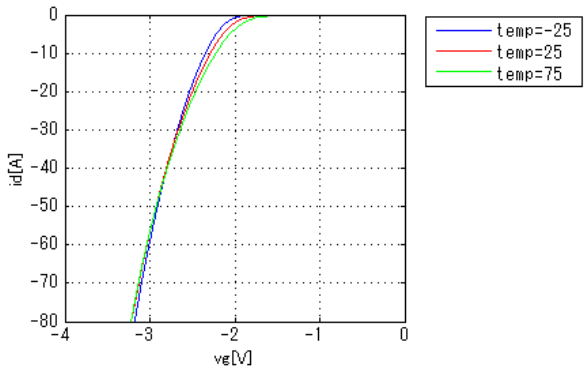
IdVds[Vgs]

Temp. = 25deg C

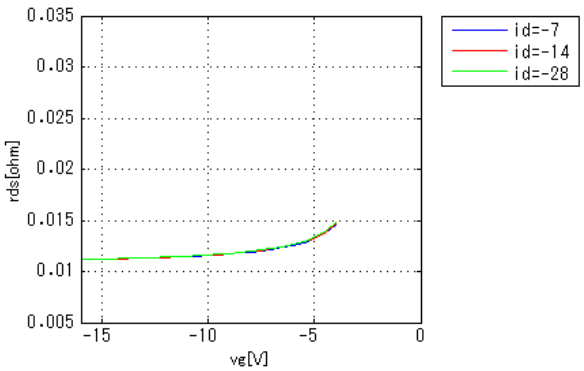


IdVgs[Temp]

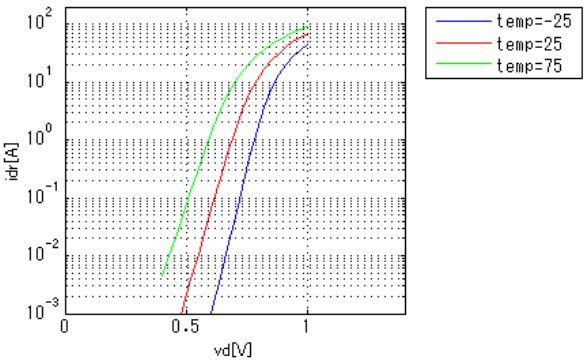
Vds = -10V



Rds(on)Vgs[Id]

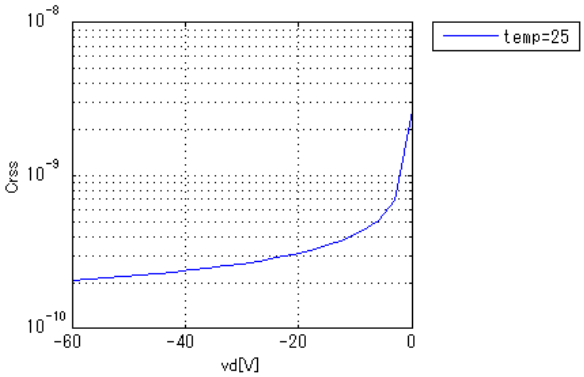


IsVsd[Temp]



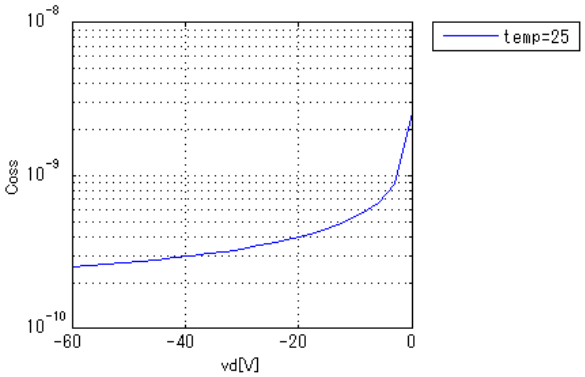
Crss

Freq. = 1MHz



Coss

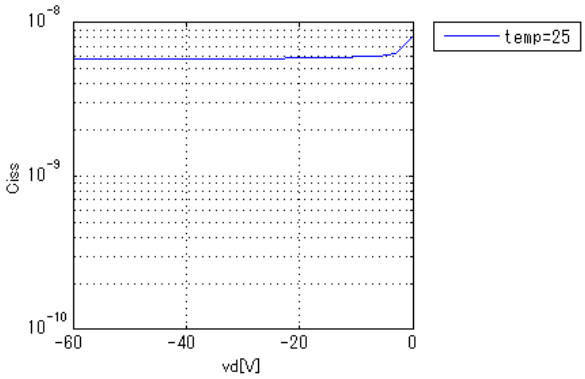
Freq. = 1MHz



Simulation results are following.
Explanatory notes — : simulated

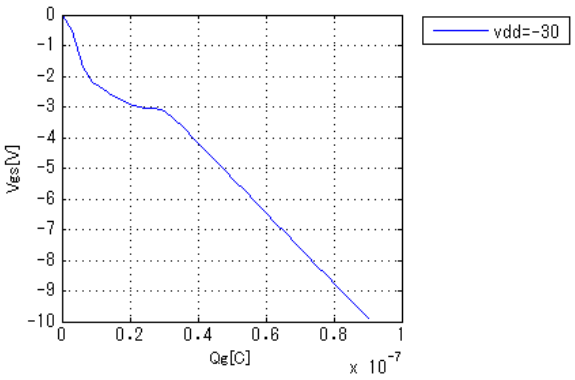
Ciss

Freq. = 1MHz



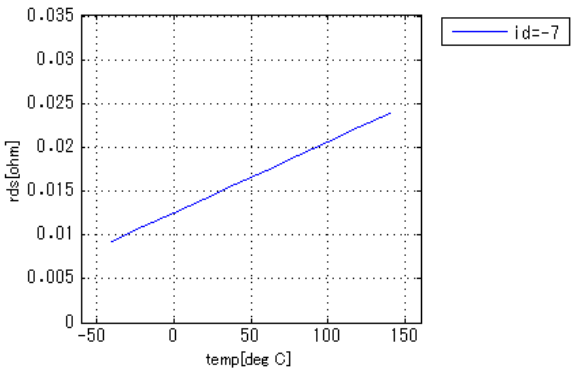
VgsQg[Vdd]

Id = -55A



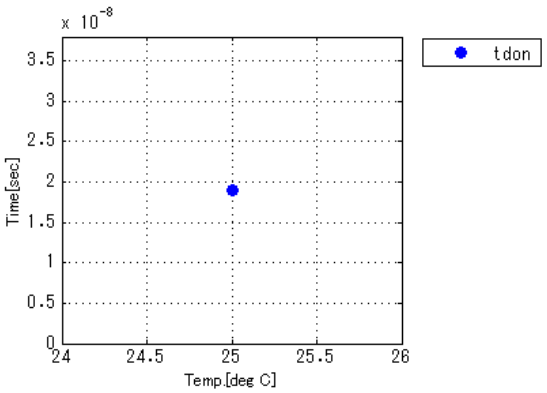
Rds(on)Temp[Id]

Vgs = -4V



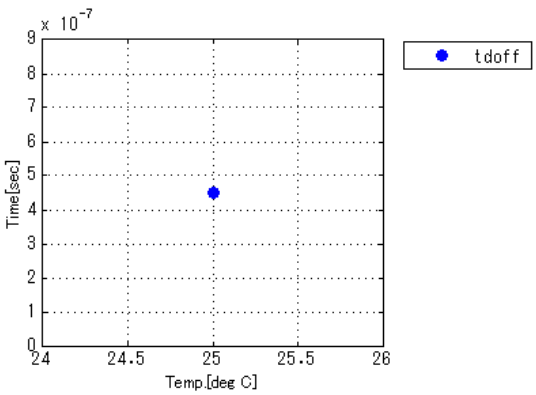
tdon

Vdd = -30V, Id = -28A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



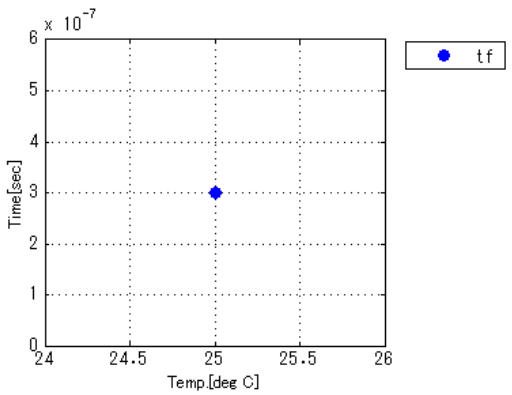
tdoff

Vdd = -30V, Id = -28A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



tf

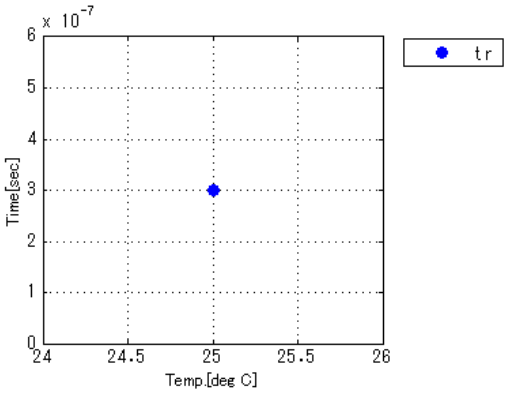
Vdd = -30V, Id = -28A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



Simulation results are following.
Explanatory notes　— : simulated

tr

Vdd = -30V, Id = -28A, +Vg = 0V, -Vg = -10V, Rg = 0.001ohm



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