

PSpice Model

Resistor-Equipped Transistor (RET)

Nexperia

PDTC114EU

Model Information

Model A macro model
Call Name MDC_PDTC114EU_PS
Pin Assign 1:BASE 2:EMITTER 3:COLLECTOR
File List Model Library MDC_PDTC114EU_PS.lib
 Model Report MDC_PDTC114EU_PS.pdf(this file)
Verified Simulator Version PSpice v17.2

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev. 12 — 21 December 2011
- Product name PDTC114E_SER
- Company name Nexperia B.V.

[Characteristics listed]

- Characteristics VCEsat-IC
hFE-IC
Cob-VR
Vlon-IC
Vloff-IC

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	-40,25,100	deg C

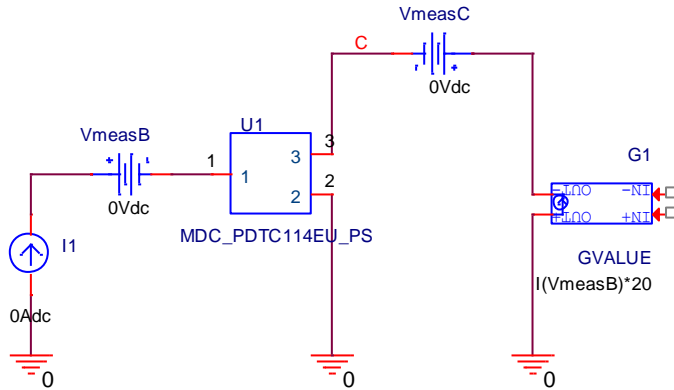
○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table
RANK=1

Functions	RANK	Implemented
VIN(on)-Iout(Temp)	1	○
Iout-VIN(off)(Temp)	1	○
Iout-Vo-Iin	1	—
DC_Current_Gain-Iout	1	○
VOOUT(on)-Iout(Temp)	1	—
VOOUT(sat)-Iin(Temp)	1	○
Capacitance	1	○
Transition Frequency	1	—
Switching(Typ.)	1	—

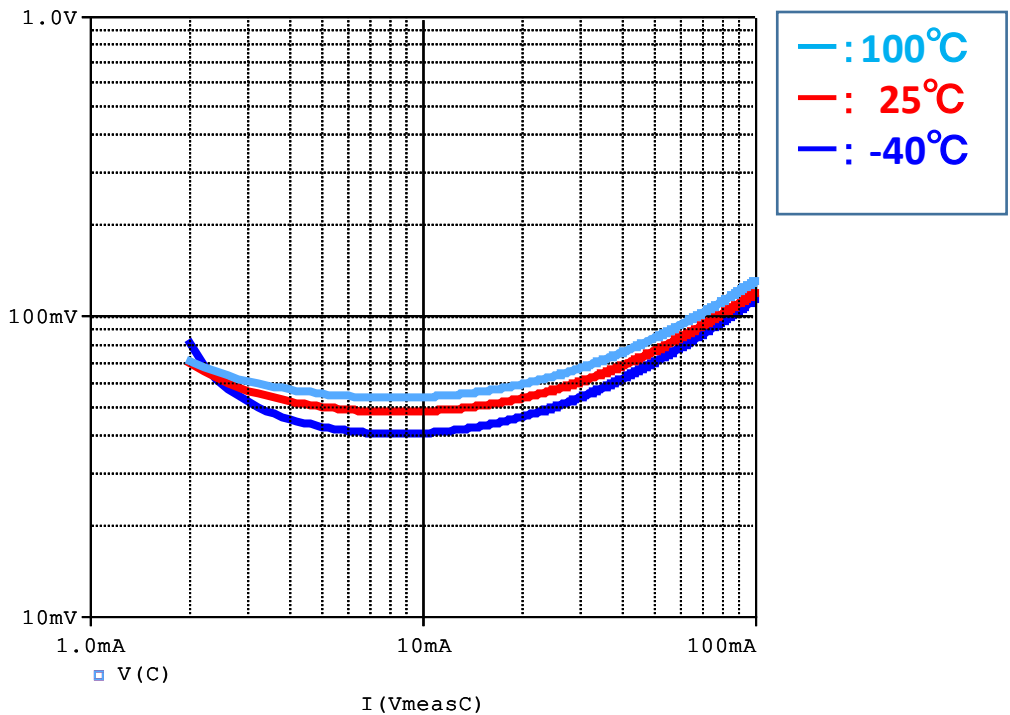
VCEsat-IC Testbench

Referred to Data Sheet



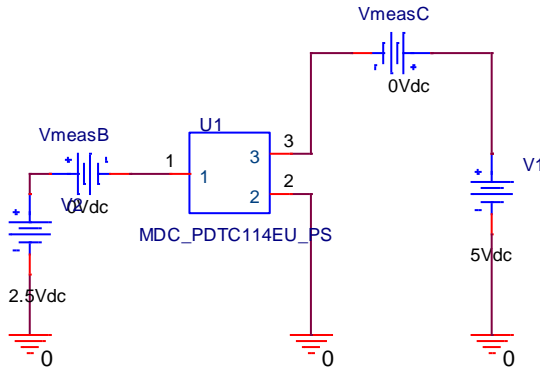
Simulation results are following.
 Explanatory notes — : simulated

VCEsat-IC



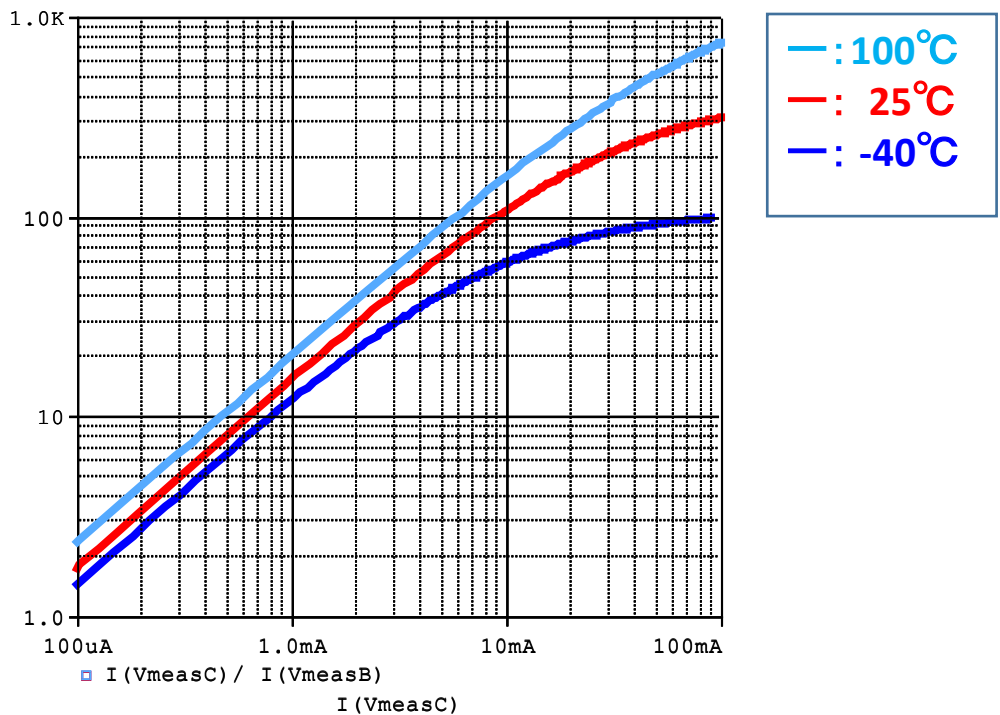
hFE-IC Testbench

Referred to Data Sheet



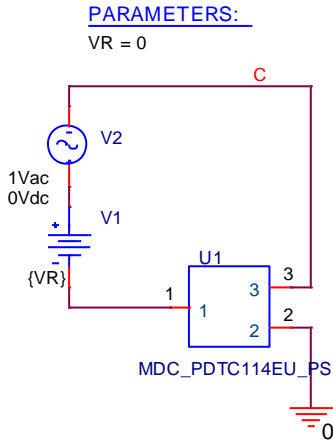
Simulation results are following.
 Explanatory notes — : simulated

hFE-IC



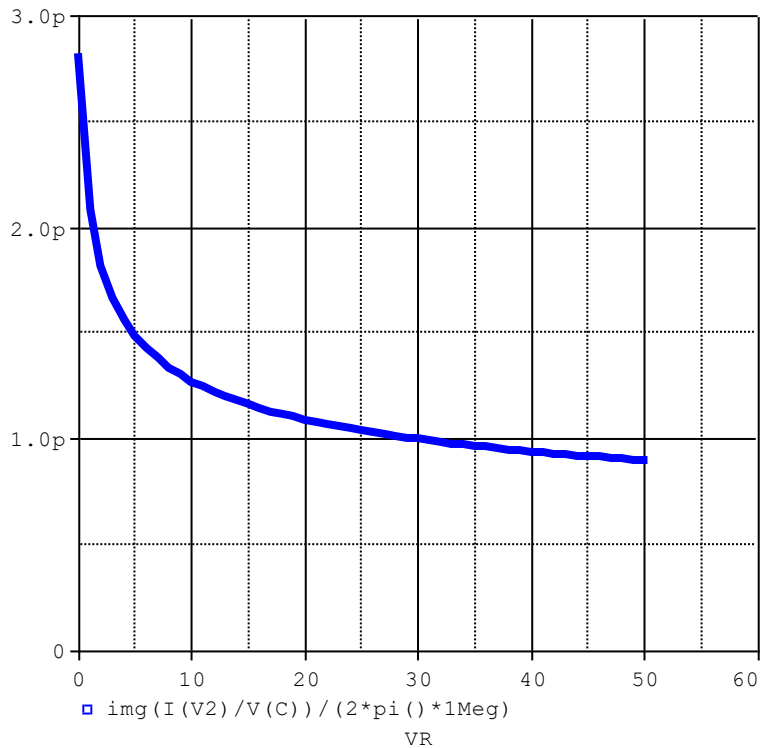
Cob-VR Testbench

Referred to Data Sheet



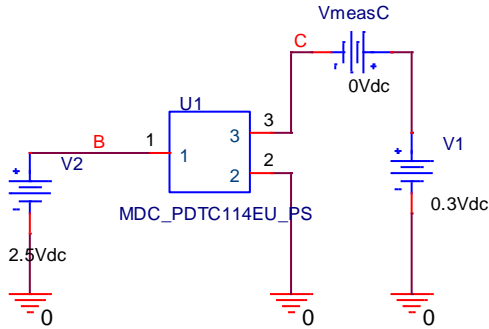
Simulation results are following.
Explanatory notes — : simulated

Cob-VR



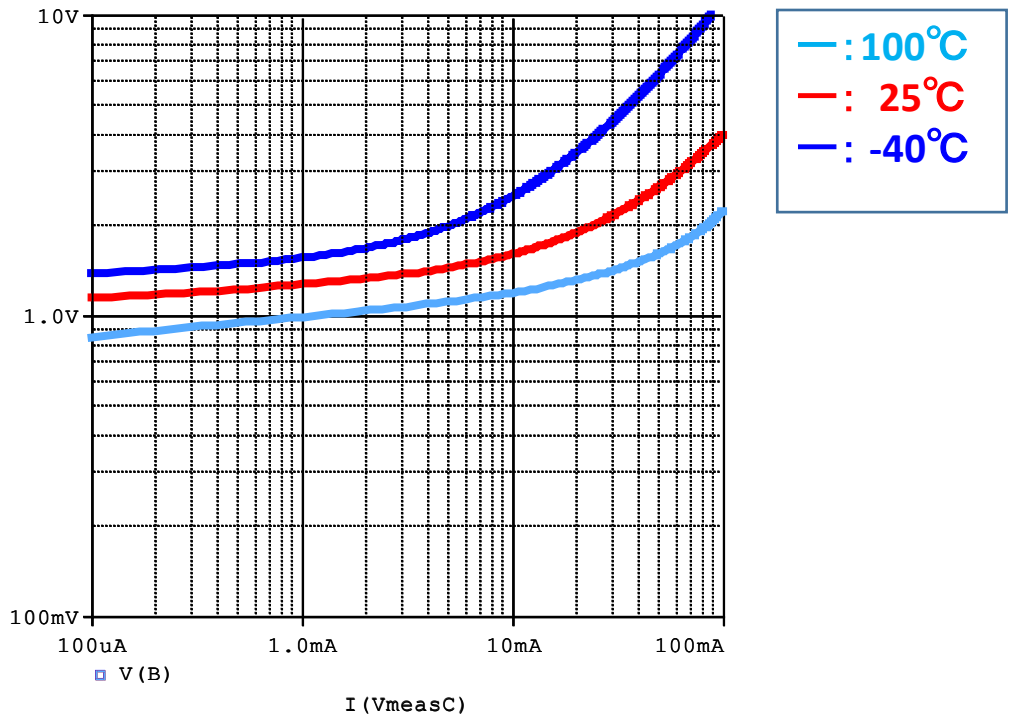
V_{lon}-IC Testbench

Referred to Data Sheet



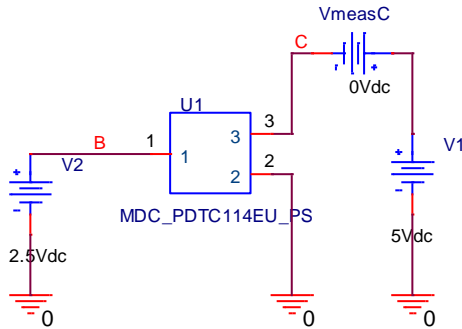
Simulation results are following.
 Explanatory notes — : simulated

V_{lon}-IC



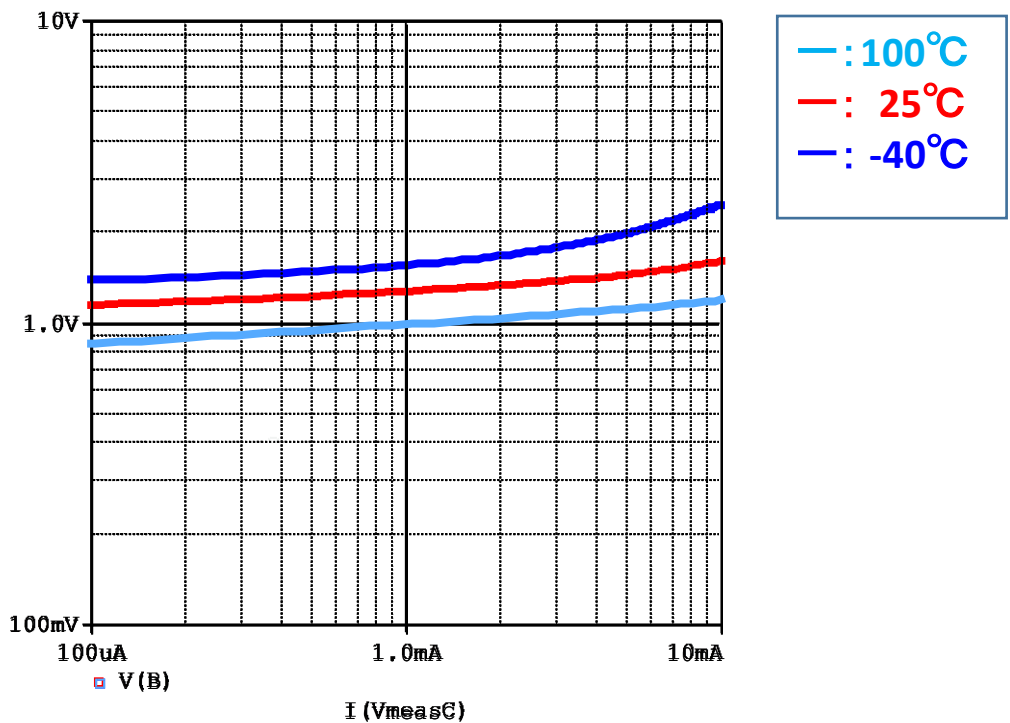
Vloff-IC Testbench

Referred to Data Sheet



Simulation results are following.
 Explanatory notes — : simulated

Vloff-IC



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