LTspice Model
LDO
Torex Semiconductor
XC6223T181MR-G

Model Information

Model	A macro model
Call Name	MDC_XC6223T181MR-G_LT
Pin Assign	1:VIN 2:VSS 3:CE 4:NC 5:VOUT
File List	Model Library MDC_XC6223T181MR-G_LT03.lib
	Model Report MDC_XC6223T181MR-G_LT.pdf(this file)

Verified Simulator Version   LTspice XVII

Note

References

The information which was used for modeling is as follow:

[Data Sheet]
- ●Date/Version   N/A
- ●Product name   XC6223T181MR-G
- ●Company name   Torex Semiconductor

[Characteristics listed]
- ●Characteristics   VIN-VOUT,Limit Current,Dropout Voltage
  Line Regulation,Load Regulation,CE

Simulation Condition

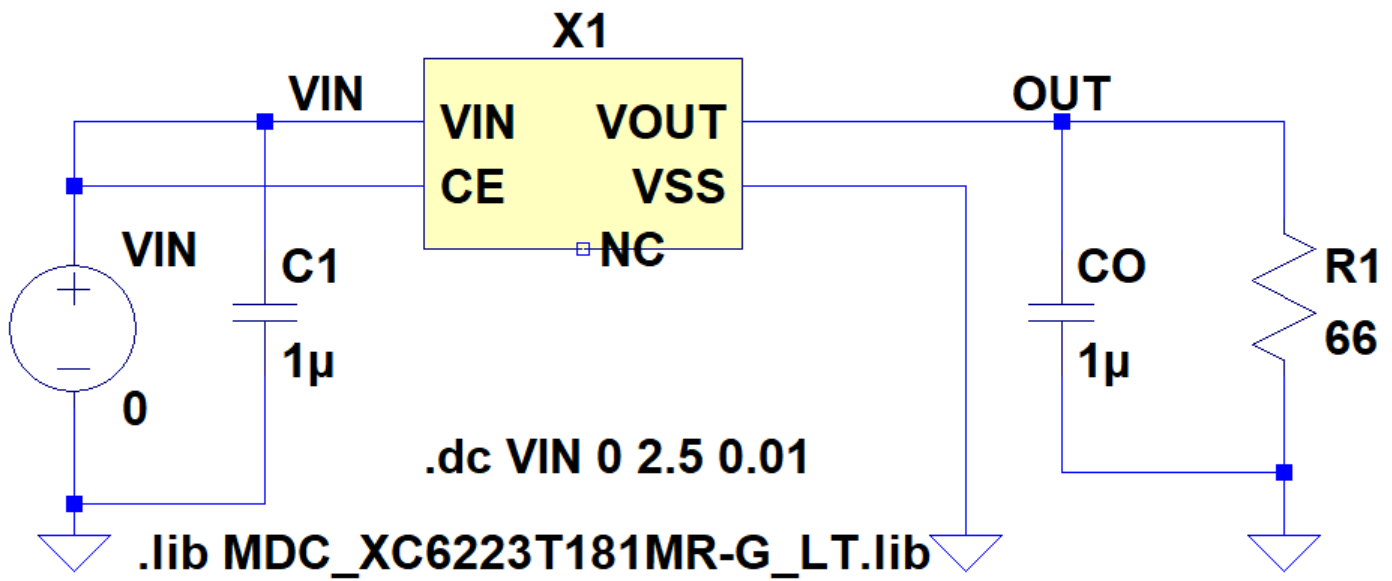This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

2

Model Functions Table

Functions	Implemented
VIN-VOUT	◯
Limit Current	◯
Dropout Voltage	◯
Line Regulation	◯
Load Regulation	◯
CE	◯

VIN-VOUT Testbench

Referred to Data Sheet

VIN

VIN   X1

VIN   VOUT   OUT

CE   VSS

NC

VIN   C1   CO   R1

1μ   1μ   66
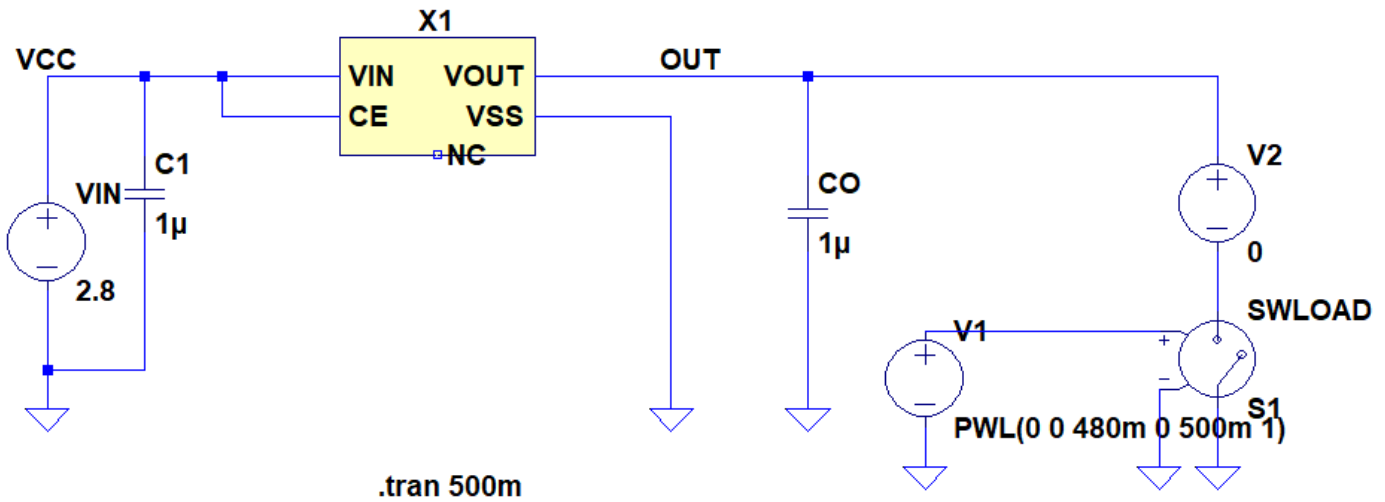
0

.dc VIN 0 2.5 0.01

.lib MDC_XC6223T181MR-G_LT.lib

Simulation results are following.
Explanatory notes   — : simulated

VIN-VOUT
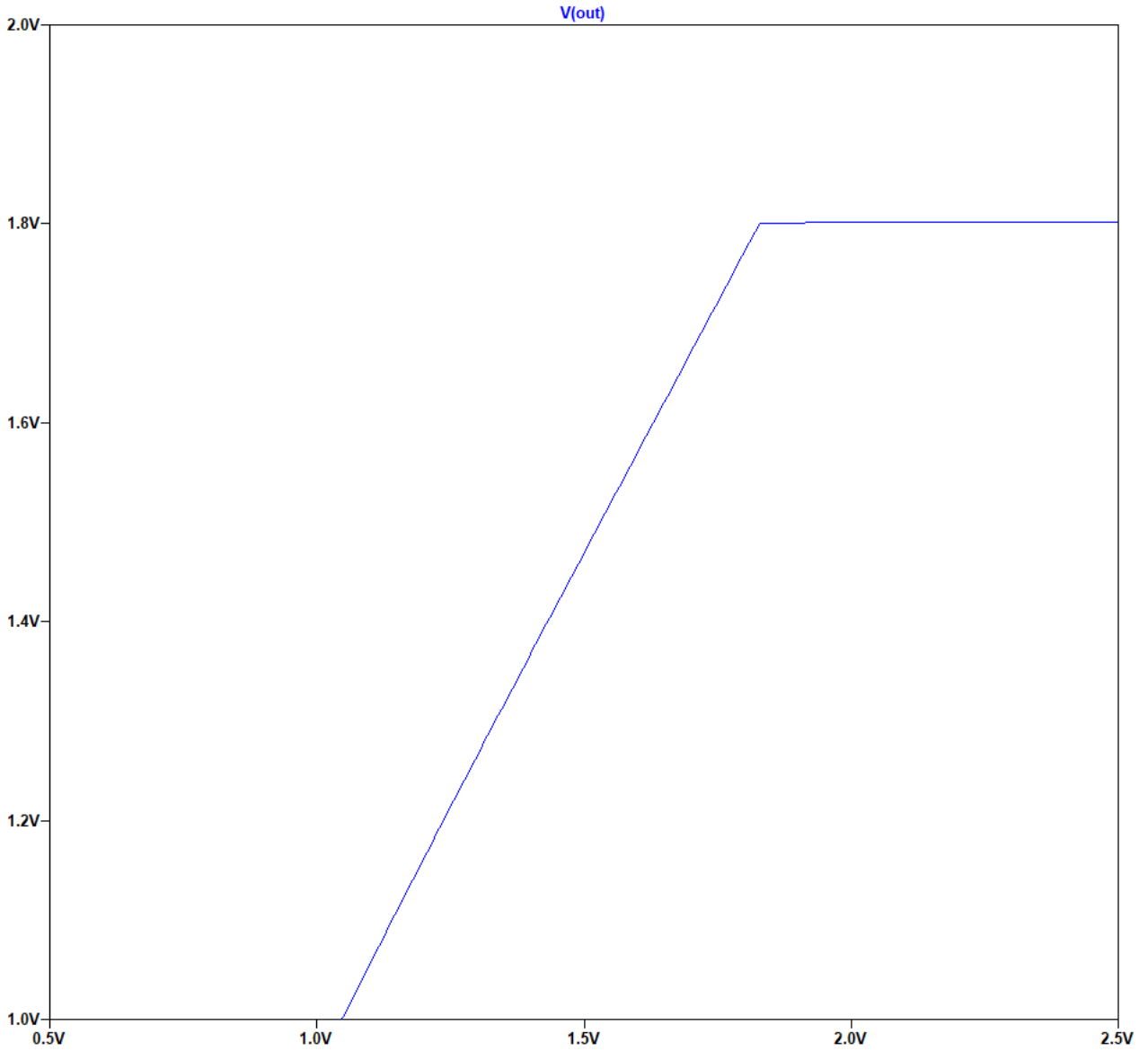
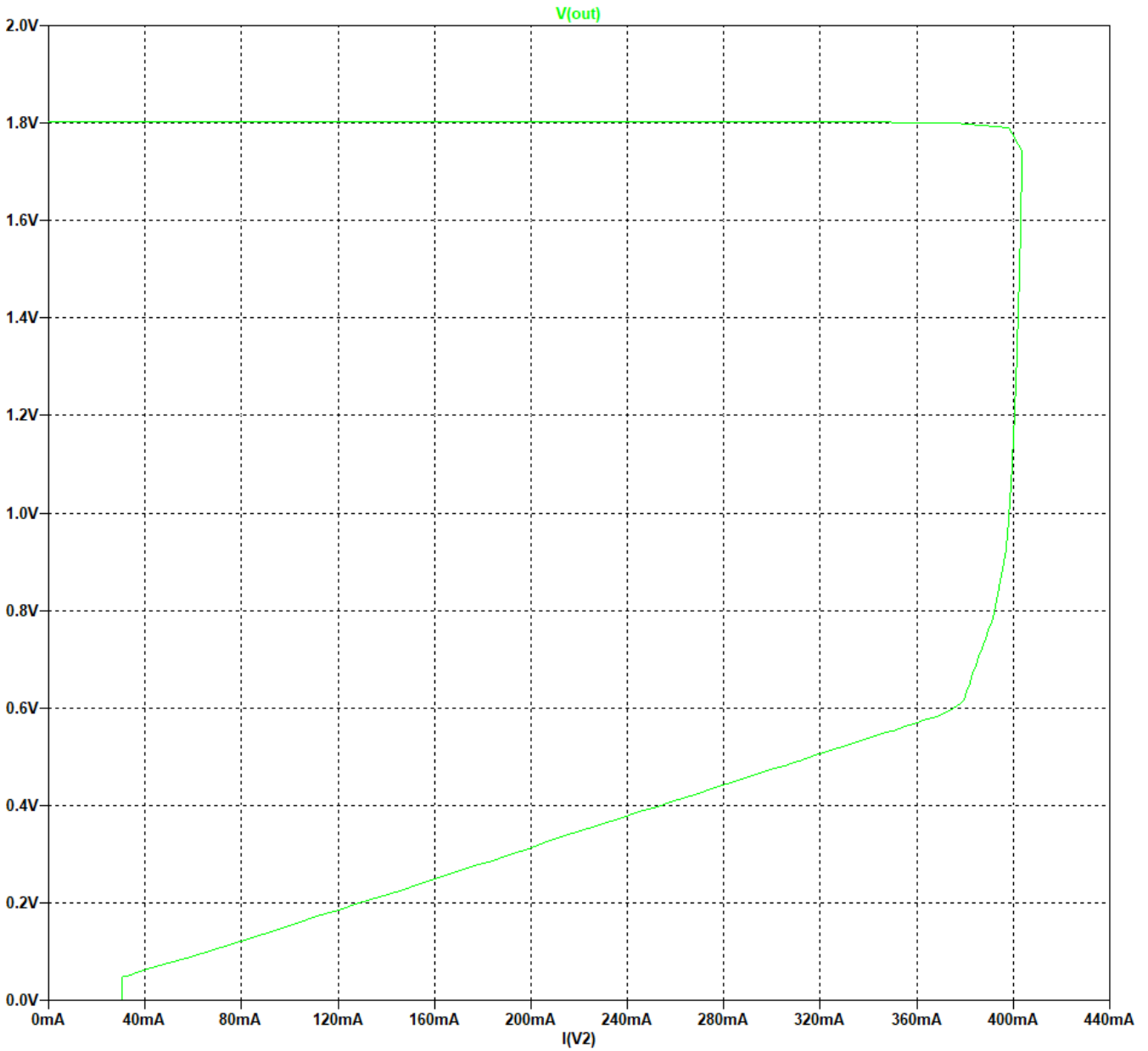**Limit Current Testbench**

Referred to Data Sheet

.tran 500m

.MODEL SWLOAD SW RON=1m ROFF=1Meg VON=1 VOFF=0
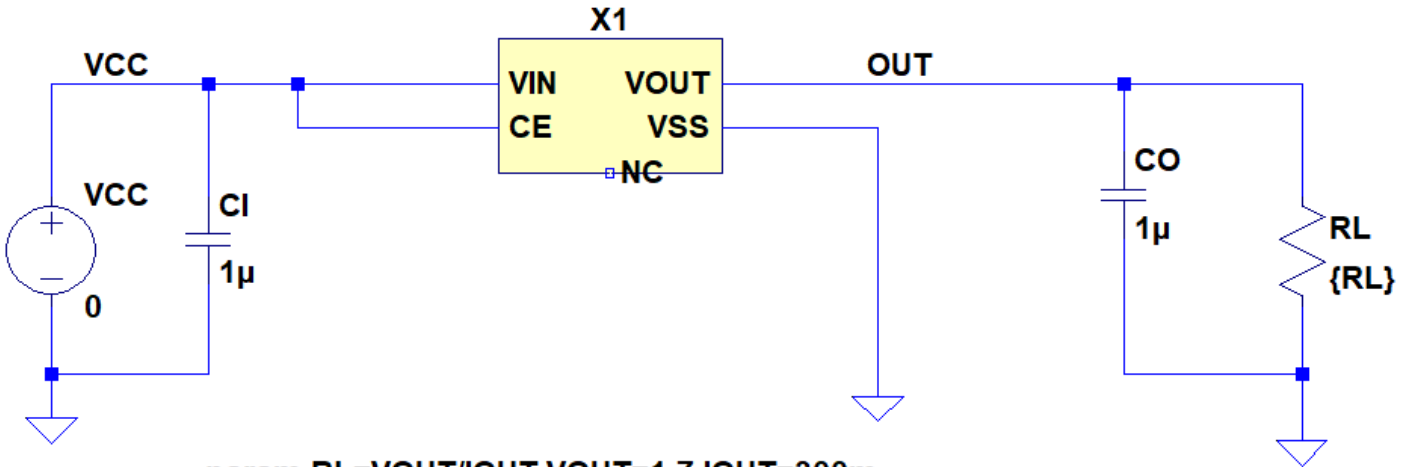.lib MDC_XC6223T181MR-G_LT.lib

Simulation results are following.
Explanatory notes   — : simulated

Limit Current

Dropout Voltage Testbench

Referred to Data Sheet

.param RL=VOUT/IOUT VOUT=1.7 IOUT=300m

.dc VCC 0 5.5 0.01
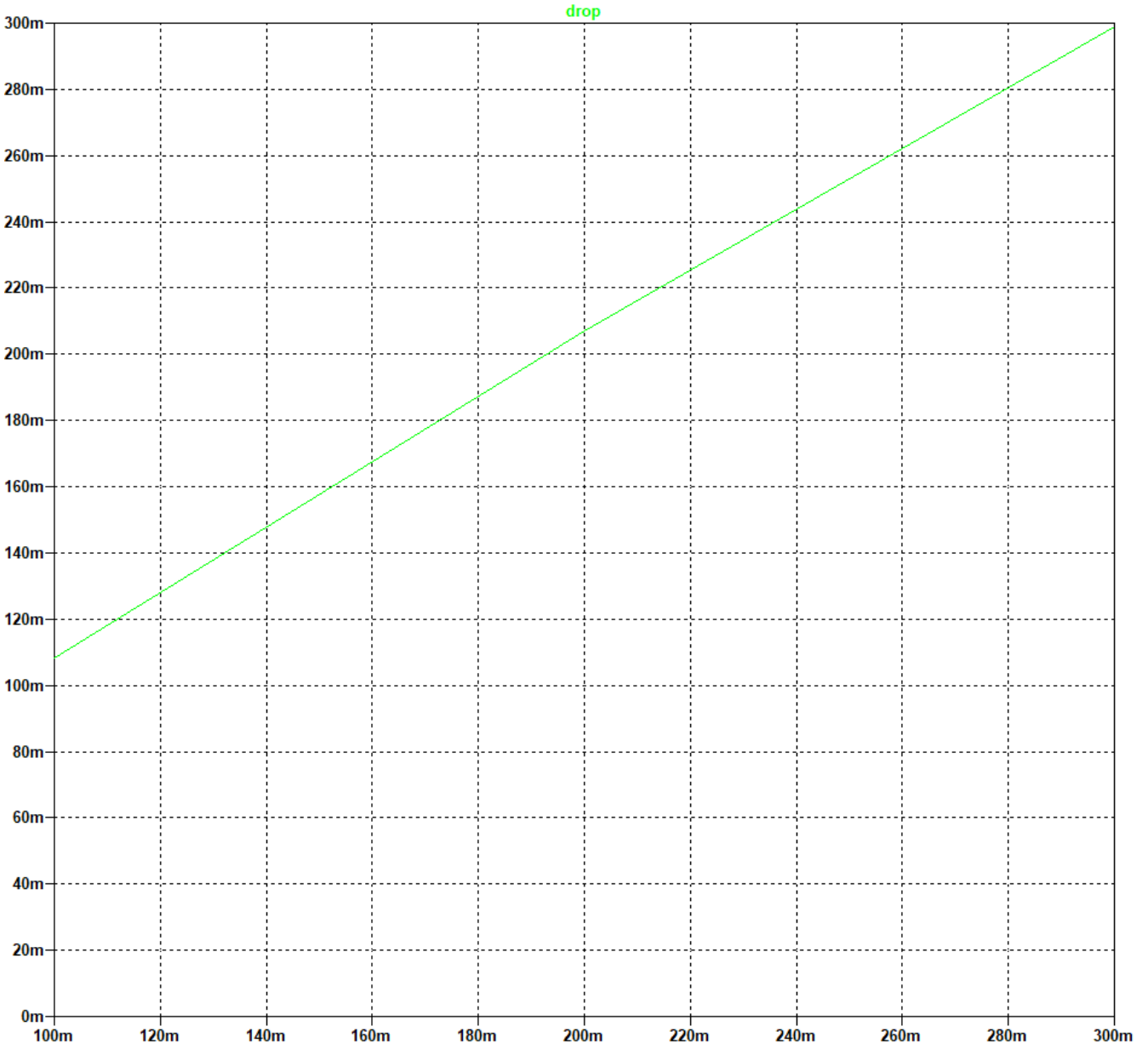
.step param IOUT 100m 300m 100m

.meas DC drop FIND V(VCC)-V(OUT) WHEN V(OUT)=1.7 RISE=1

.lib MDC_XC6223T181MR-G_LT.lib

Simulation results are following.
Explanatory notes   — : simulated

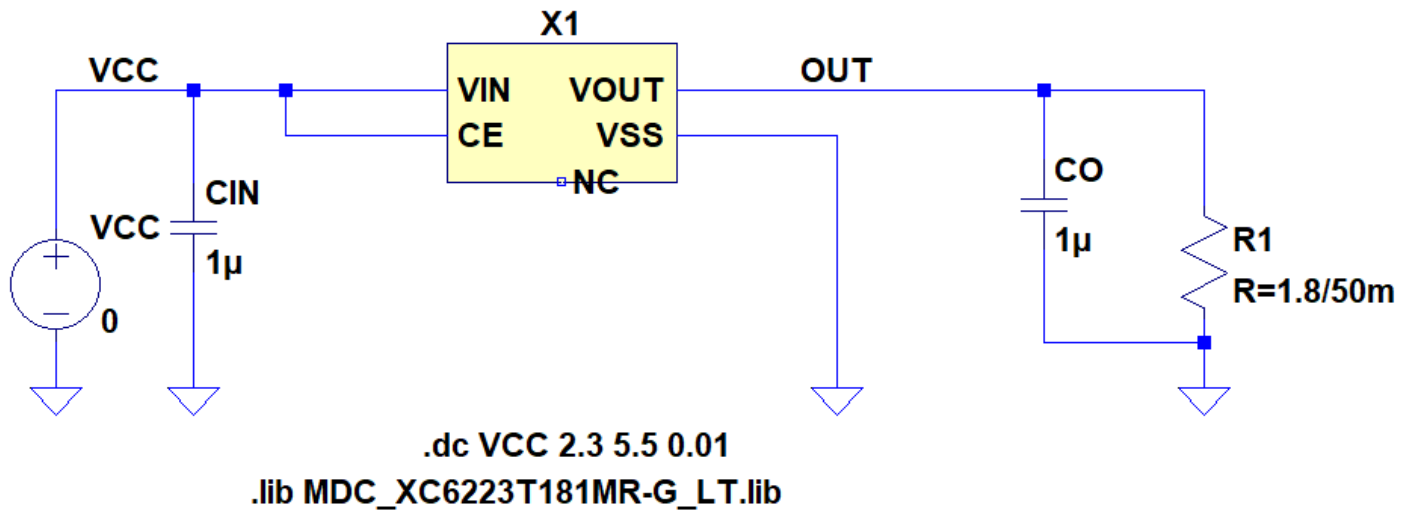**Dropout Voltage**

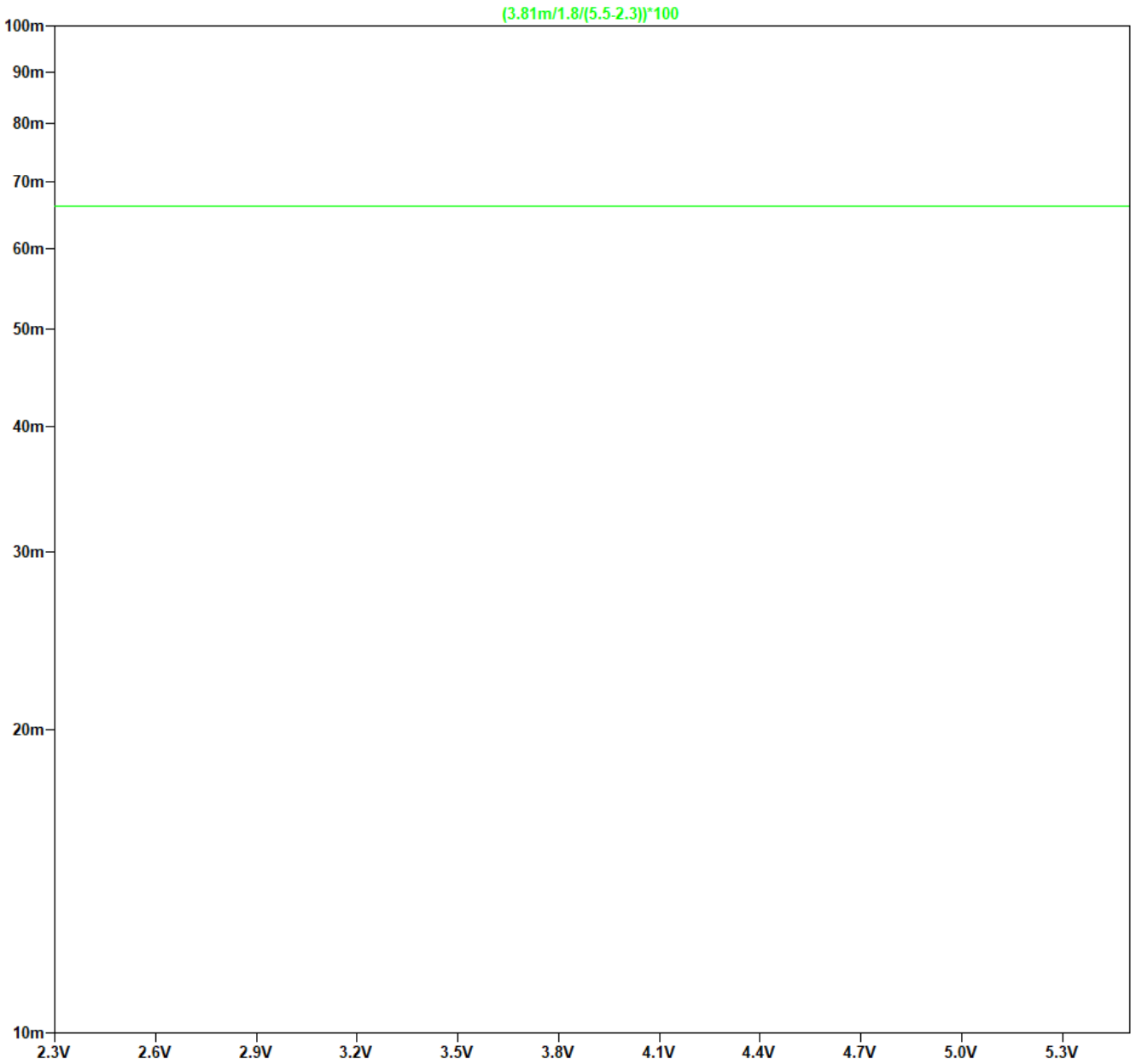**Line Regulation** Testbench

Referred to Data Sheet
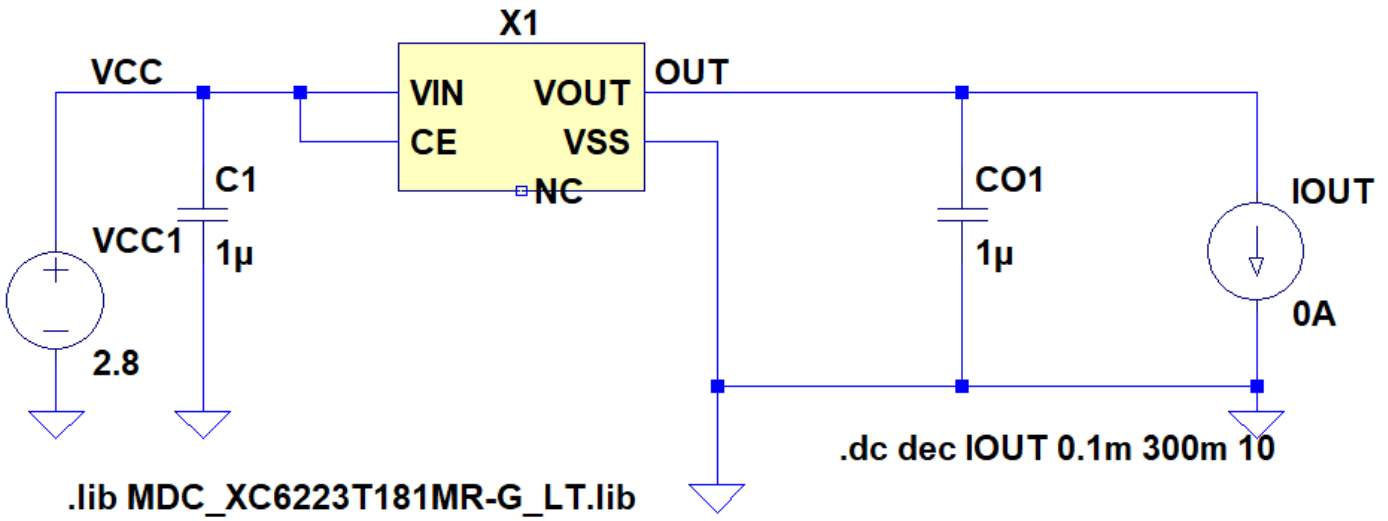

.dc VCC 2.3 5.5 0.01
.lib MDC_XC6223T181MR-G_LT.lib

Simulation results are following.
Explanatory notes　　—　: simulated
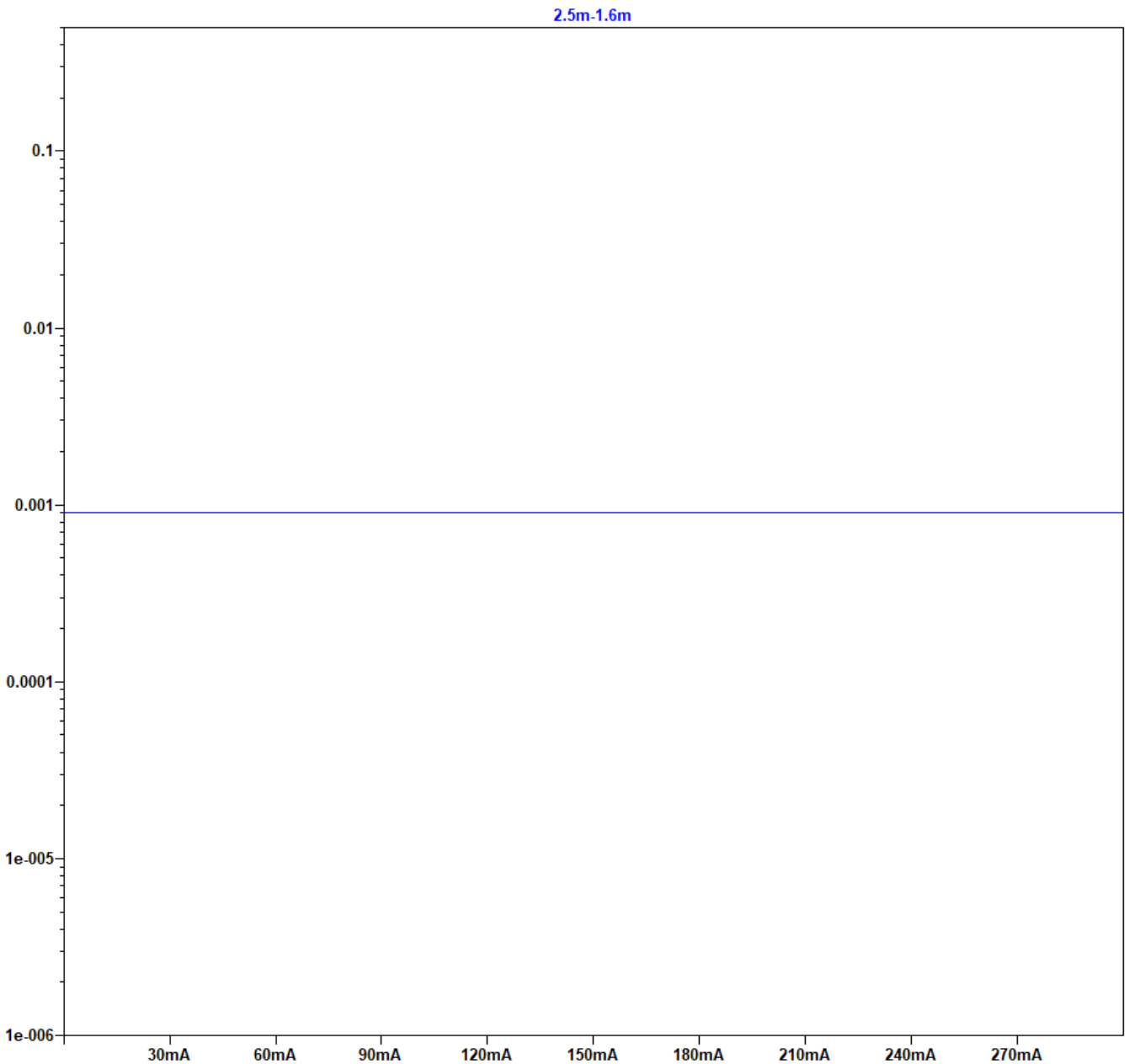
Line Regulation

(3.81m/1.8/(5.5-2.3))*100

Load Regularion Testbench

Referred to Data Sheet
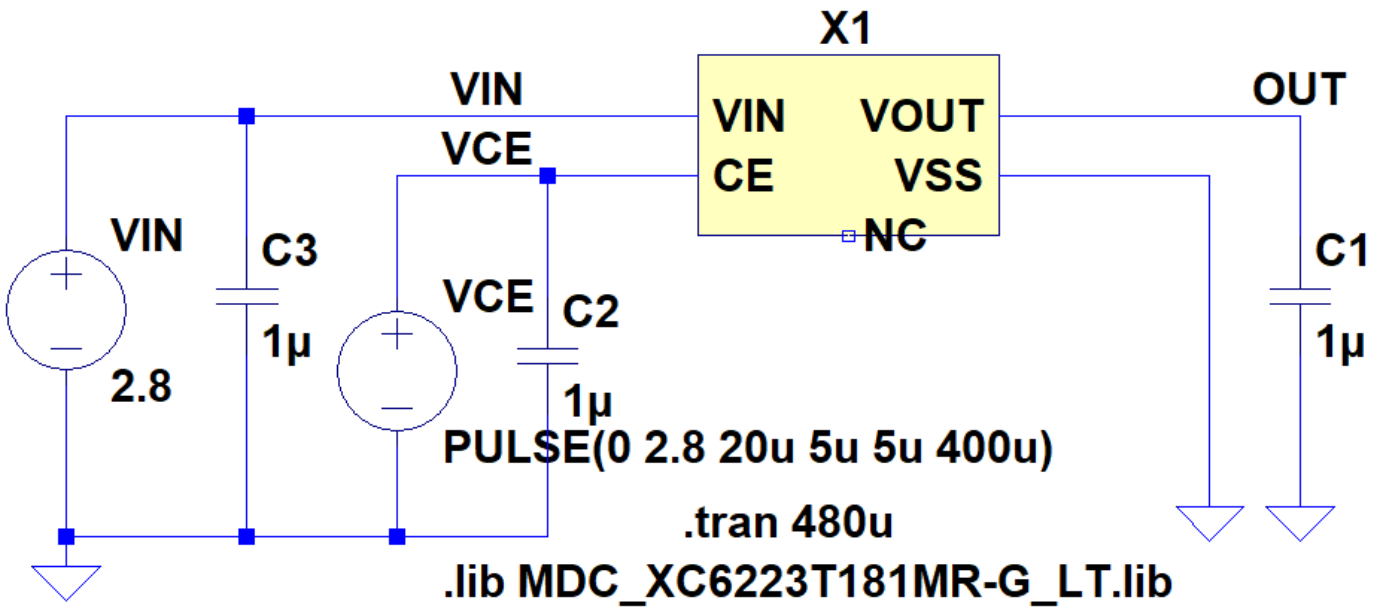
Simulation results are following.
Explanatory notes　　— : simulated

Load Regulation

2.5m-1.6m

CE Testbench

Referred to Data Sheet

X1

VIN
VCE

VIN   VOUT
CE   VSS
            NC

OUT

VIN
2.8

C3
1µ

VCE
C2
1µ

C1
1µ

PULSE(0 2.8 20u 5u 5u 400u)

.tran 480u

.lib MDC_XC6223T181MR-G_LT.lib

Simulation results are following.
Explanatory notes ― : simulated

CE
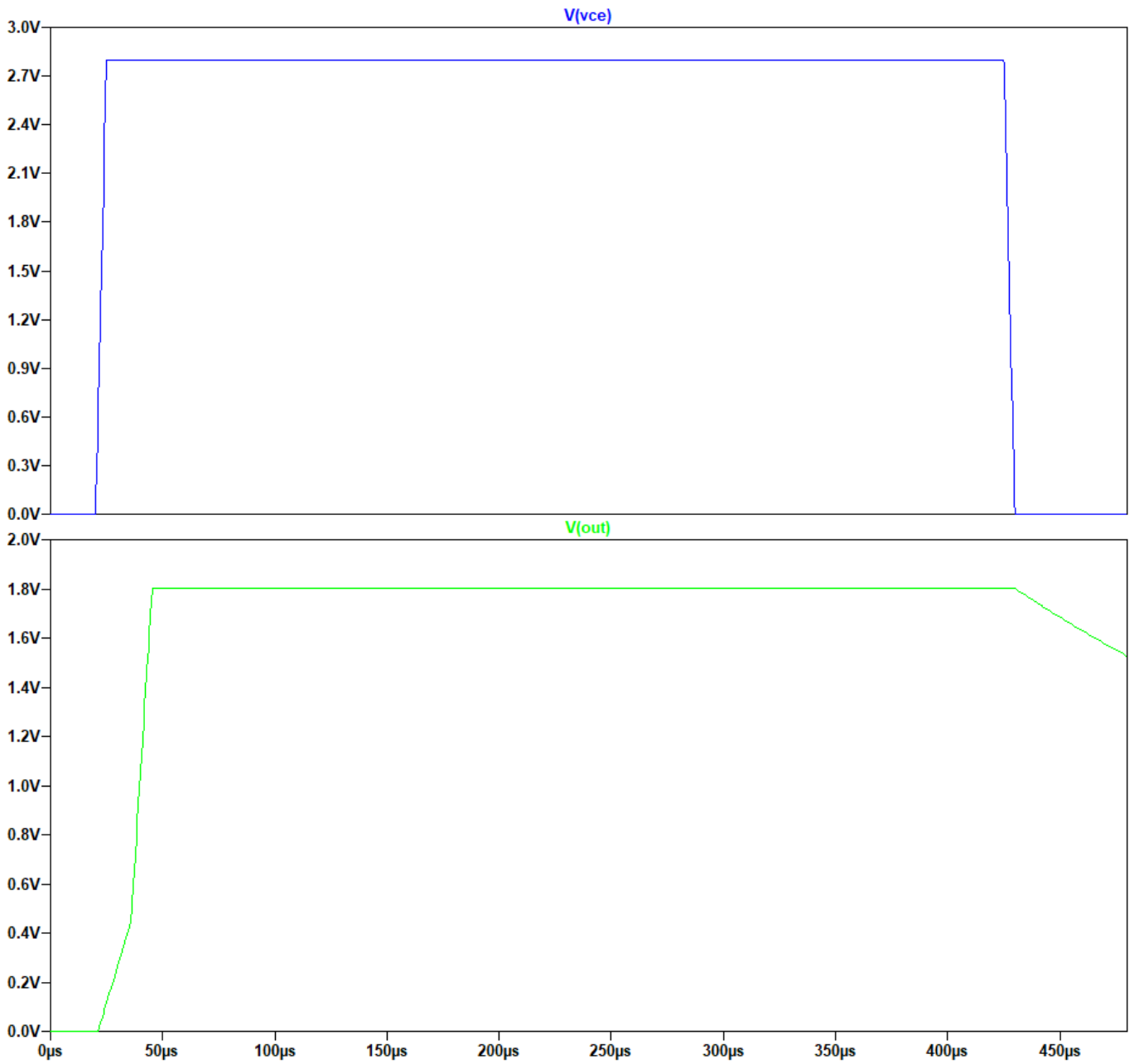
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MoDeCH

Modeling Design Technology

MoDeCH Inc.

Head Office
Location: 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan
Tel:+81-42-656-3360
E-Mail:model-on-support@modech.co.jp
URL:http://www.modech.com/en/

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