

MDC_IRFB4410PBF_LT

LTspice Model NMOS Infineon IRFB4410PBF

Model Information

| Model Call Name | A macro model based on BSIM3 model MDC_IRFB4410PBF_LT | | |
|--------------------|--|--|--|
| Pin Assign | 1:D 2:G 3:S | | |
| File List | Model Library Model Report | MDC_IRFB4410PBF_LT01.lib MDC_IRFB4410PBF_LT.pdf (this file) | |

Verified Simulator Version Note

LTspice version XVII

References

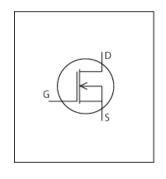
The information which was used for modeling is as follow:

01/31/06 IRFB4410PBF Infineon Technologies AG IdVds[Vgs],IdVds[Vgs]02,IdVgs[Temp],Rds(on)Temp[Id],Cap acitanceVds[Cname],VgsQg[Vdd],IsVsd[Temp],BvTemp[ir],V thTemp[Id],SwitchingIdd[Tname],Trrlf[Ir],Qrrlf[Ir],SwitchingW aveform,TrrQrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item | Range | | | Unit |
|---------------------------|-------|----|------|-------|
| | Min. | | Max. | |
| Drain-source voltage (DC) | 0 | to | 100 | V |
| Gate-source voltage (DC) | -20 | to | 20 | V |
| Temperature | -55 | to | 175 | deg C |

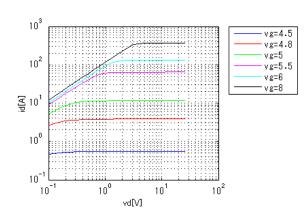




Simulation results are following. Explanatory notes -: simulated

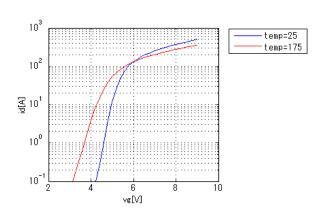
ldVds[Vgs]

Temp. = 25degC



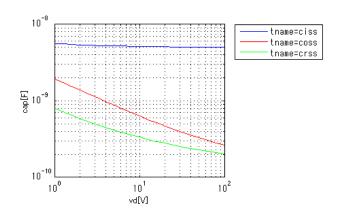
ldVgs[Temp]

Vds = 25V



CapacitanceVds[Cname]

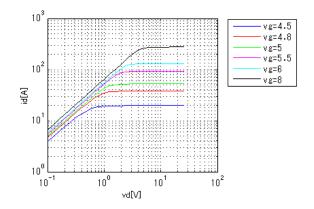
freq = 1000000Hz



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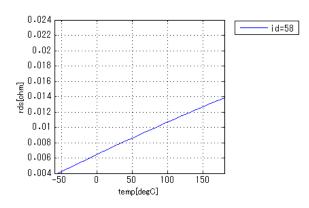
ldVds[Vgs]02

Temp. = 175degC



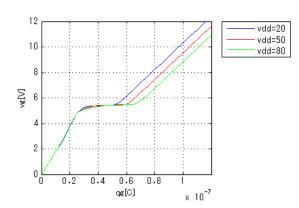
Rds(on)Temp[Id]

Vgs = 10V



VgsQg[Vdd]

ld = 58A

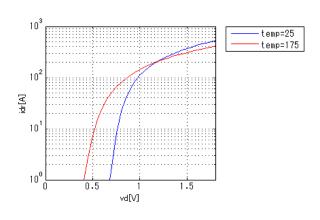




Simulation results are following. Explanatory notes — : simulated

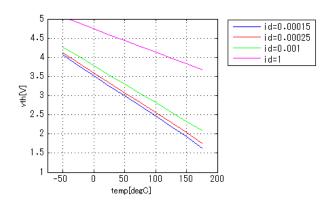
IsVsd[Temp]





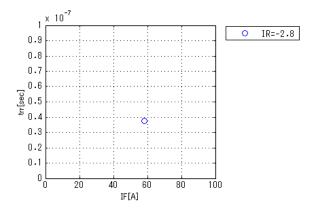
VthTemp[Id]

Vd = Vg



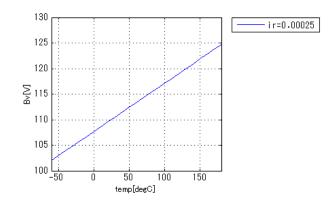
Trrlf[lr]

vdd = 85V, didt = 100A/us



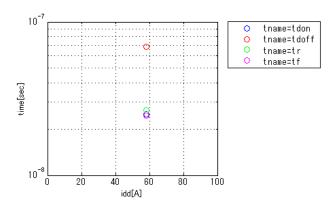
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BvTemp[ir]

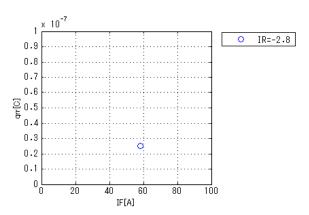


SwitchingIdd[Tname]

vgg = 10V, vdd = 65V, RGG = 4.1ohm



Qrrlf[lr] vdd = 85V, didt = 100A/us

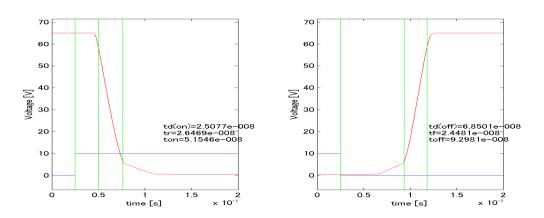




Simulation results are following. Explanatory notes — : simulated

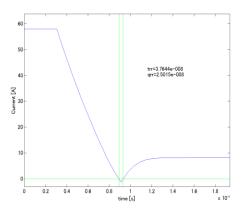
SwitchingWaveform

Blue : INPUT Red : OUTPUT



TrrQrrWaveform

vdd = 85V, didt = 100A/us





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MoDeCH Inc.

Head Office Location: Taiju-Seimei-Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan Tel:+81-42-656-3360 E-Mail:model-on-support@modech.co.jp URL:http://www.modech.com/en/