MDC_RT1N141M_PS



PSpice Model BRT (Bias Resistor Transistor) Isahaya RT1N141M

Model Information

 Model
 A macro model based on Gummel-Poon model

 Call Name
 MDC_RT1N141M_PS

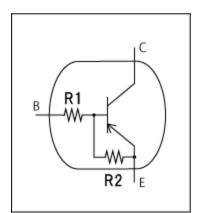
 Pin Assign
 1:B 2:E 3:C

 File List
 Model Library
 MDC_RT1N141M_PS02.lib

 Model Report
 MDC_RT1N141M_PS.pdf (this file)

Verified Simulator Version Note

PSpice version 17.2



References

The information which was used for modeling is as follow:

[Data Sheet]
Date/Version
Product name
Company name
Characteristics

2016/11 RT1N141M Isahaya Electronics Corporation hFEIc[Temp],VionIc[Temp],IcVioff[Temp],Vce(sat)Ic[Temp],f TIe[Vce]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
R1	10,000	to	10,000	ohm
R2	10,000	to	10,000	ohm
Temperature	-55	to	150	deg C

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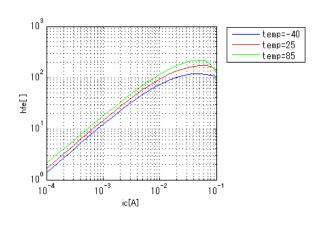
BRT Model Functions Table		O : Implemented × : Not Implemented — : Not applicable	
	RANK=1		
Functions	RANK	Implemented	
VIN(on)-Iout(Temp)	1	0	
Iout-VIN(off)(Temp)	1	0	
hFE-Ic(Temp)	1	0	
Vce(sat)-Ic(Temp)	1	0	
Capacitance	1	—	
Transition Frequency	1	0	
Switching(Typ.)	1	—	



Simulation results are following. Explanatory notes -: simulated

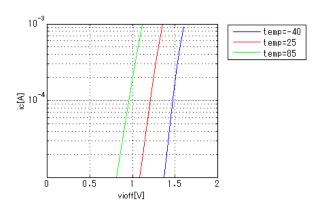
hFElc[Temp]

Vce = 5V



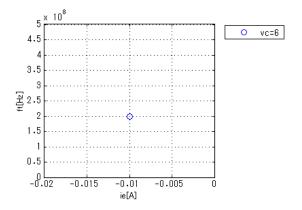
IcVioff[Temp]

Vce = 5V



fTle[Vce]

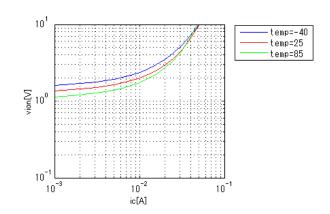
Freq = 2000000Hz



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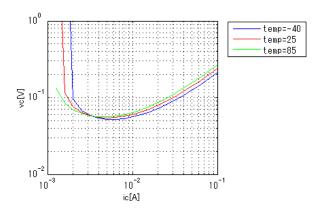
Vionlc[Temp]

Vce = 0.2V



Vce(sat)lc[Temp]

IC/IB = 20





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