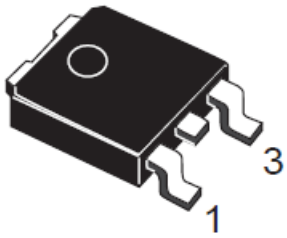
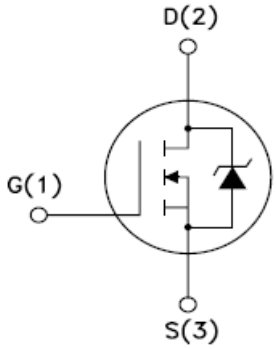
LTspice Model
NMOS
STM
STD35NF06L





Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_STD35NF06L_LT	
Pin Assign	1:G 2:D 3:S	
File List	Model Library	MDC_STD35NF06L_LT01.lib
	Model Report	MDC_STD35NF06L_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version: November 2003
- ●Product name: STD35NF06L
- ●Company name: STMicroelectronics N.V.
- ●Characteristics: IdVds[Vgs],IdVgs[Temp],YfsId[Temp],Rds(on)Id[Vgs],VgsQg[Vdd],CapacitanceVds[Cname],NormVthTemp[Id],NormRds(on)Temp[Vgs],VsdIs[Temp],SwitchingIdd[Tname],TrrIf[Ir],QrrIf[Ir],SwitchingWaveform,TrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	-16	to	16	V
Temperature	-55	to	175	deg C

MOSFET

○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table

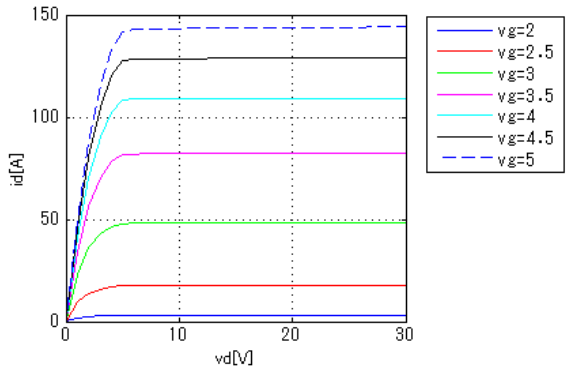
RANK=1

Functions	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS(Temp)	1	○
RDS(on)	1	○
Capacitance	1	○
Gate Charge	1	○
IS-VSD(Forward)	1	○
Reverse recovery	1	○
Switching(Typ.)	1	○
Bv	1	—
Yfs	1	○
Vth	1	○

Simulation results are following.
Explanatory notes — : simulated

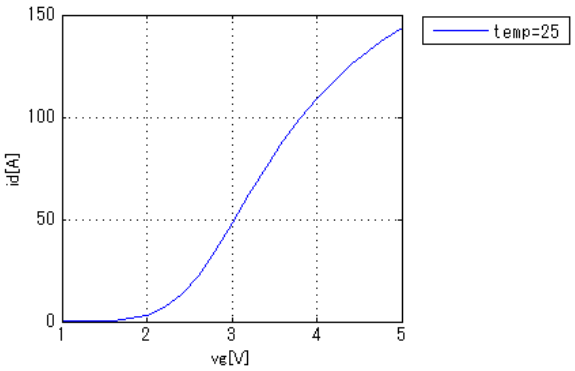
IdVds[Vgs]

Temp = 25degC



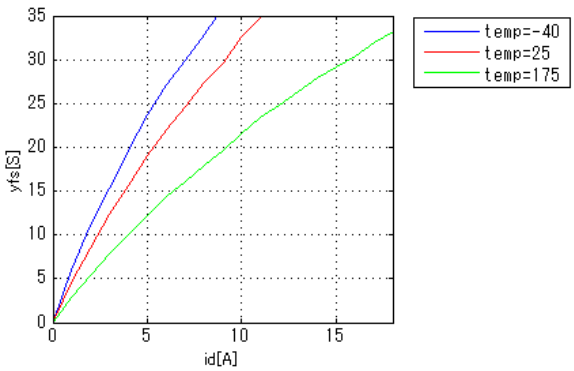
IdVgs[Temp]

Vds = 25V



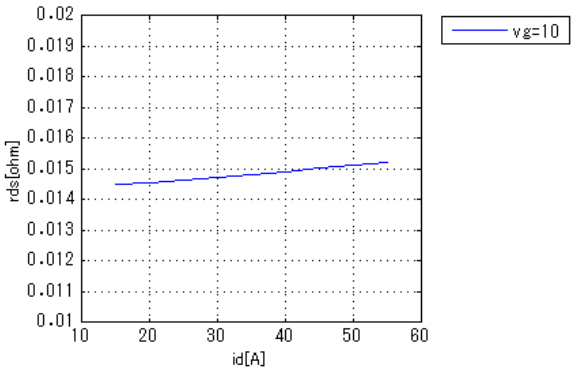
YfsId[Temp]

Vds = 15V



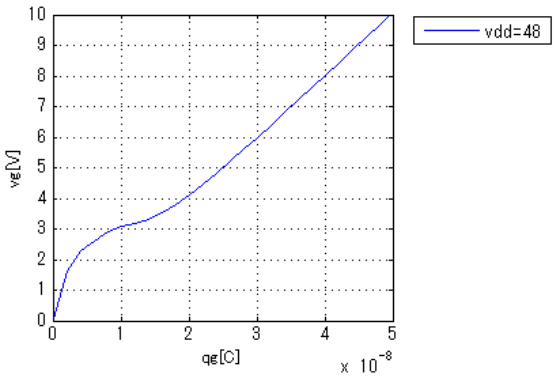
Rds(on)Id[Vgs]

Temp = 25degC



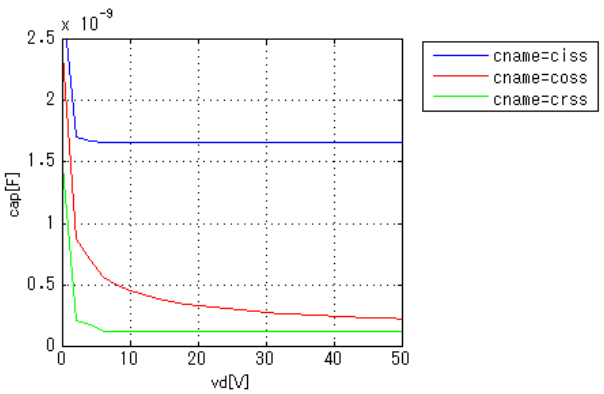
VgsQg[Vdd]

Id = 55A



CapacitanceVds[Cname]

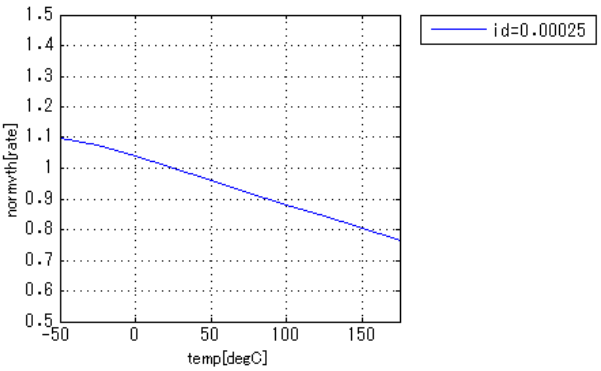
freq = 1000000Hz



Simulation results are following.
Explanatory notes — : simulated

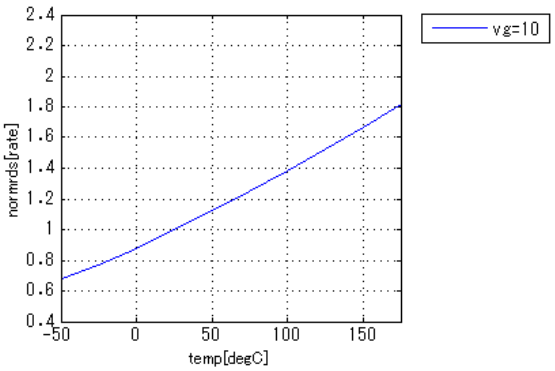
NormVthTemp[Id]

Vd = Vg



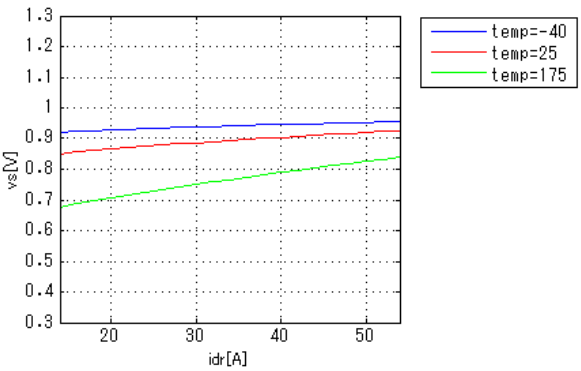
NormRds(on)Temp[Vgs]

Id = 27.5A



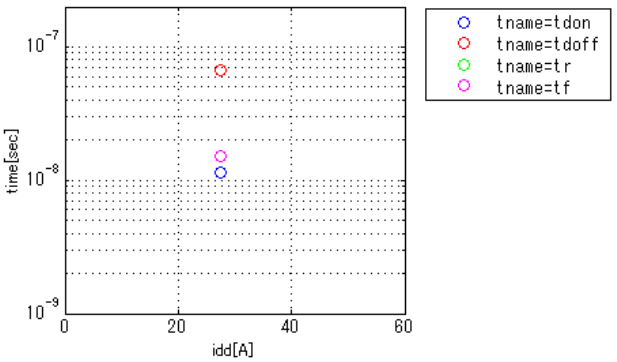
VsdIs[Temp]

vg = 0V



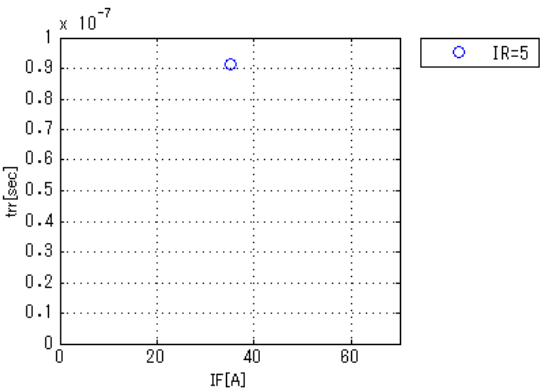
SwitchingIdd[Tname]

vgg = 4.5V, vdd = 30V, RGG = 4.7ohm



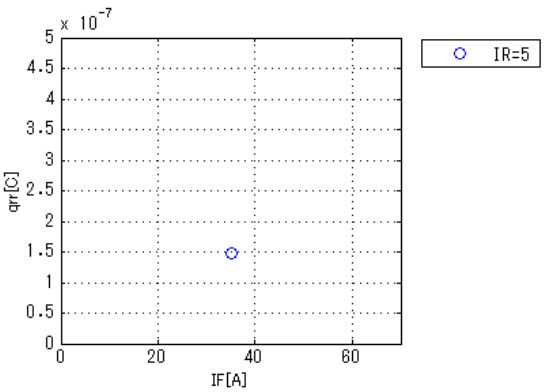
TrrIf[Ir]

vdd = 30V, didt = 100A/us, Temp = 150degC



QrrIf[Ir]

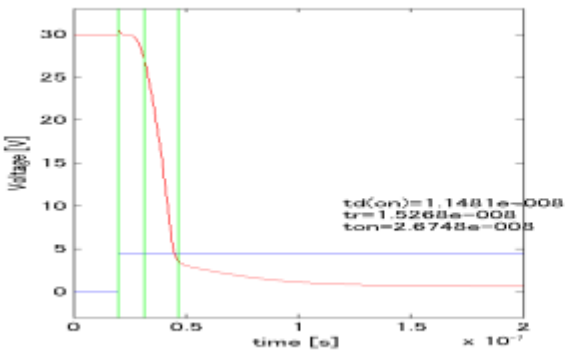
vdd = 30V, didt = 100A/us, Temp = 150degC

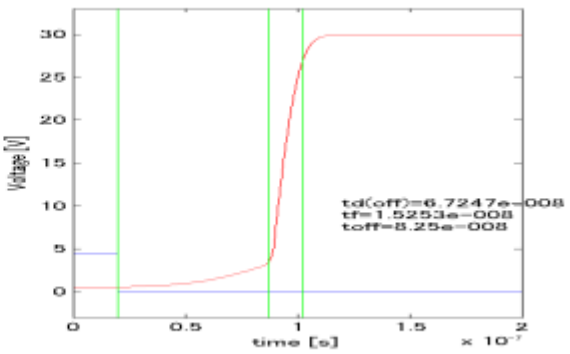


Simulation results are following.
Explanatory notes — : simulated

Switching Waveform (Blue : INPUT Red : OUTPUT)

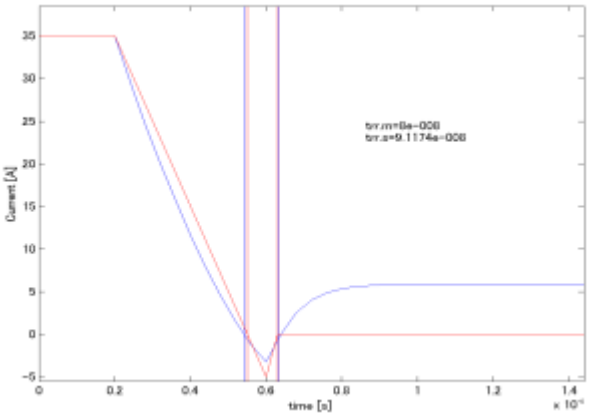
vgg = 4.5V, vdd = 30V, RGG = 4.7ohm, idd = 27.5A





Trr Waveform (Red : DATASHEET Blue : SIMULATION)

vdd = 30V, didt = 100A/us, Temp = 150degC, IF = 35A, IR = 5A



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