

# LTspice Model

## DC-DC Converter

### Texas Instruments Inc.

### UC1825J

#### Model Information

**Model** A macro model  
**Call Name** MDC\_UC1825J\_LT  
**Pin Assign** 1:INV 2:NI 3:E/AOut 4:Clock 5:RT 6:CT 7:Ramp 8:SoftStart 9:ILIM/SD 10:Gnd  
 11:OutA 12:PwrGnd 13:Vc 14:OutB 15:Vcc 16:VREF5.1V  
**File List** Model Library MDC\_UC1825J\_LT01.lib  
 Model Report MDC\_UC1825J\_LT\_LT.pdf(this file)  
**Verified Simulator Version** LTspice version XVII

#### Note

#### References

The information which was used for modeling is as follow:

[Data Sheet]  
 ● Date/Version REVISED MARCH 2004  
 ● Product name UC1825J  
 ● Company name Texas Instruments Inc.

[Characteristics listed]  
 ● Characteristics  $V_{REF}$ , SoftStart, Current Limit,  
 Shutdown, UVLO  
 $V_{OUT}$

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

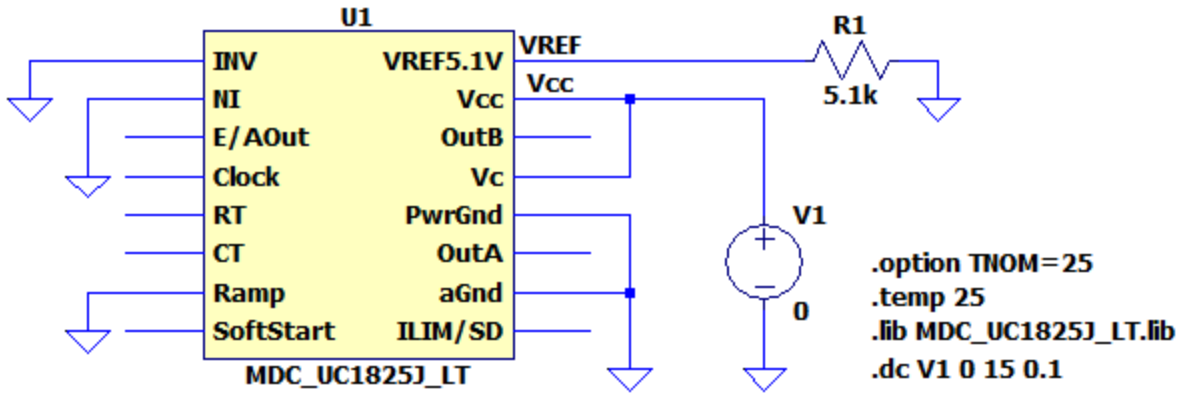
| Item        | Condition | Unit  |
|-------------|-----------|-------|
| Temperature | 25        | deg C |

**Model Functions Table**

| Functions     | Implemented |
|---------------|-------------|
| $V_{REF}$     | ○           |
| SoftStart     | ○           |
| Current Limit | ○           |
| Shutdown      | ○           |
| UVLO          | ○           |
| $V_{OUT}$     | ○           |

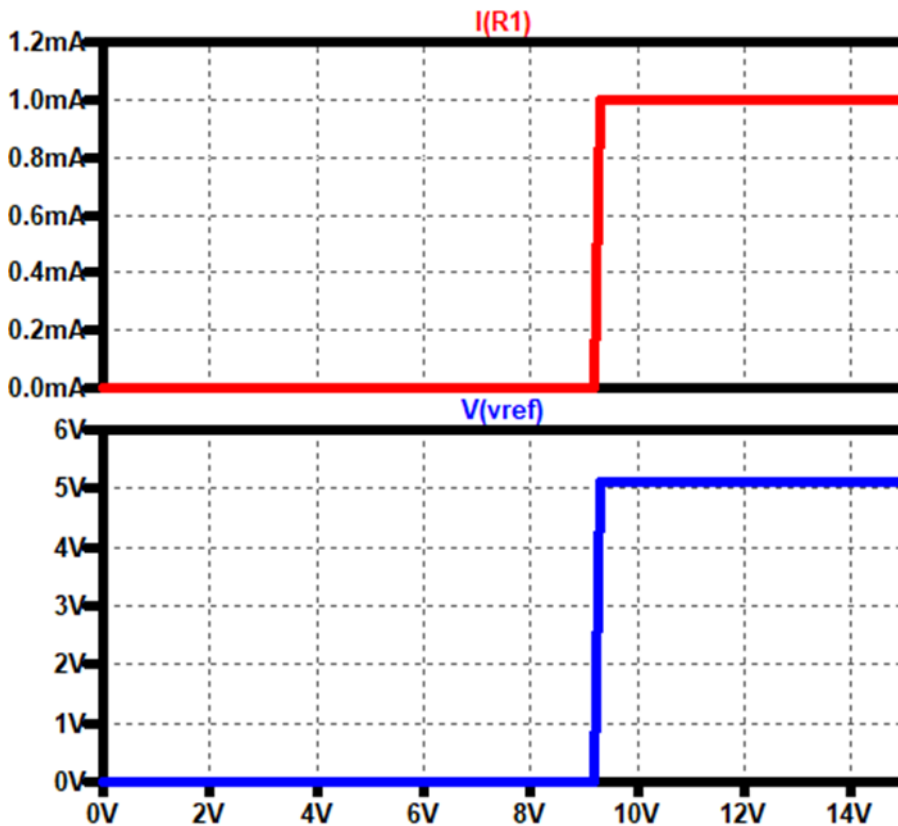
V<sub>REF</sub> Testbench

Referred to Data Sheet



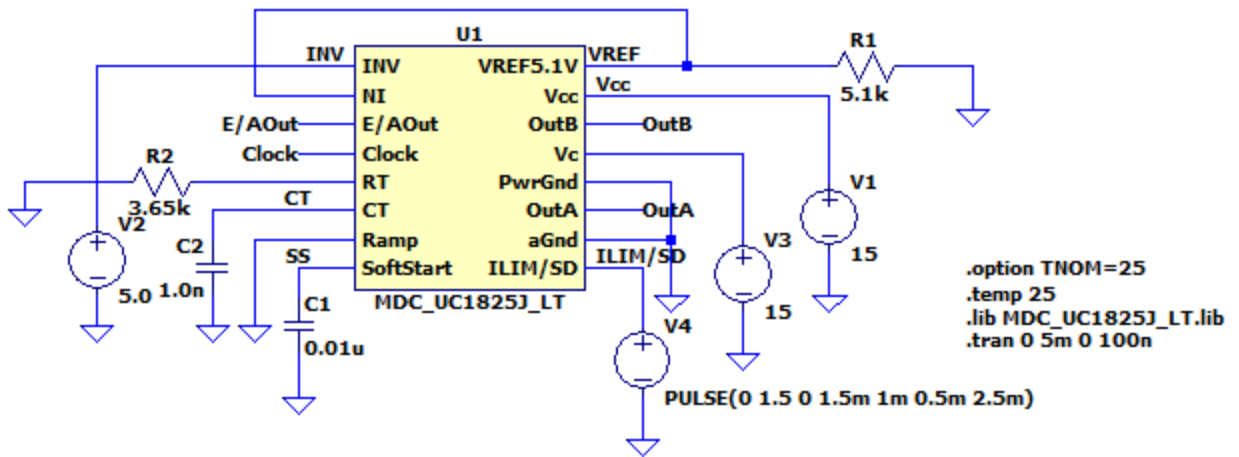
Simulation results are following.  
 Explanatory notes — : simulated

V<sub>REF</sub>



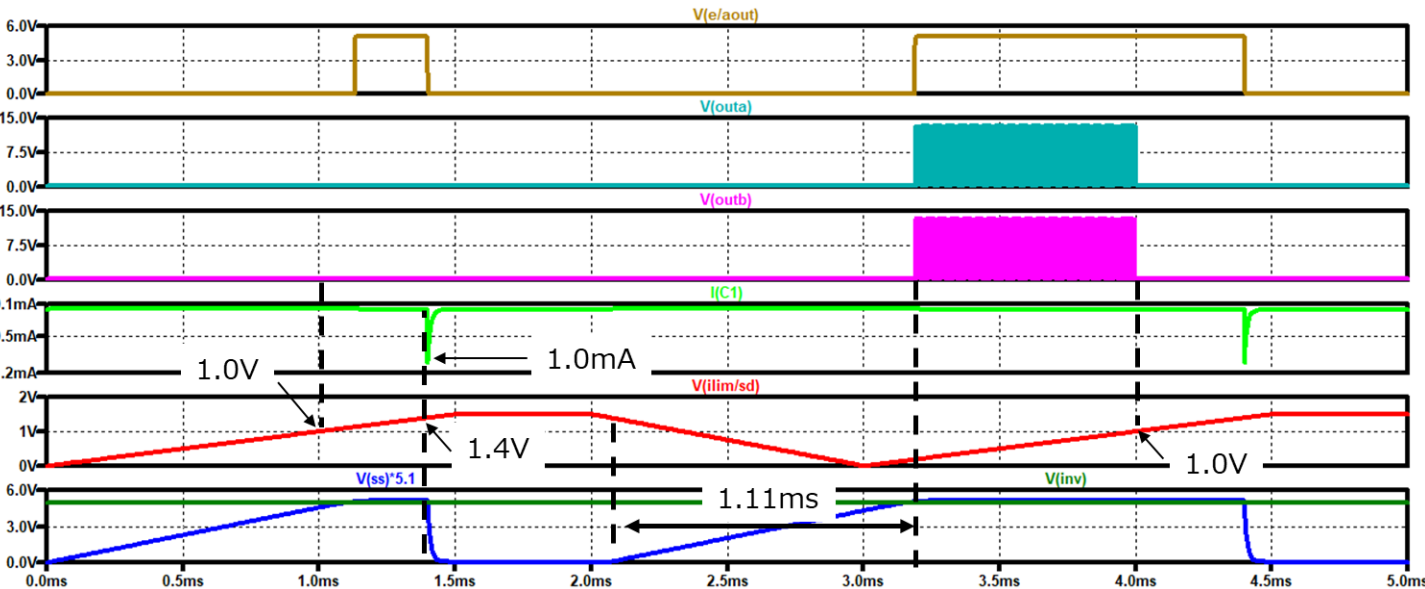
SoftStart / Current Limit / Shutdown Testbench

Referred to Data Sheet



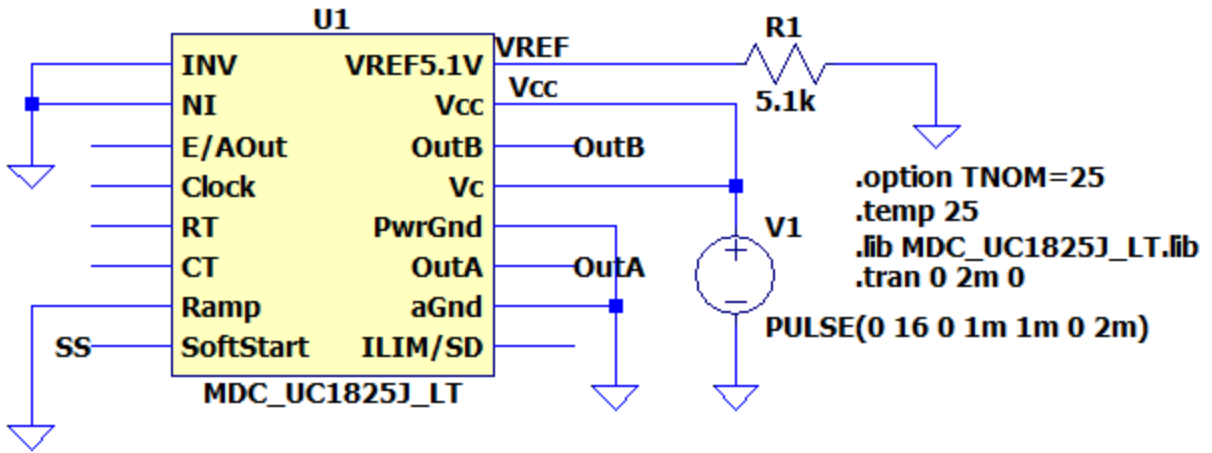
Simulation results are following.  
Explanatory notes — : simulated

SoftStart / Current Limit / Shutdown



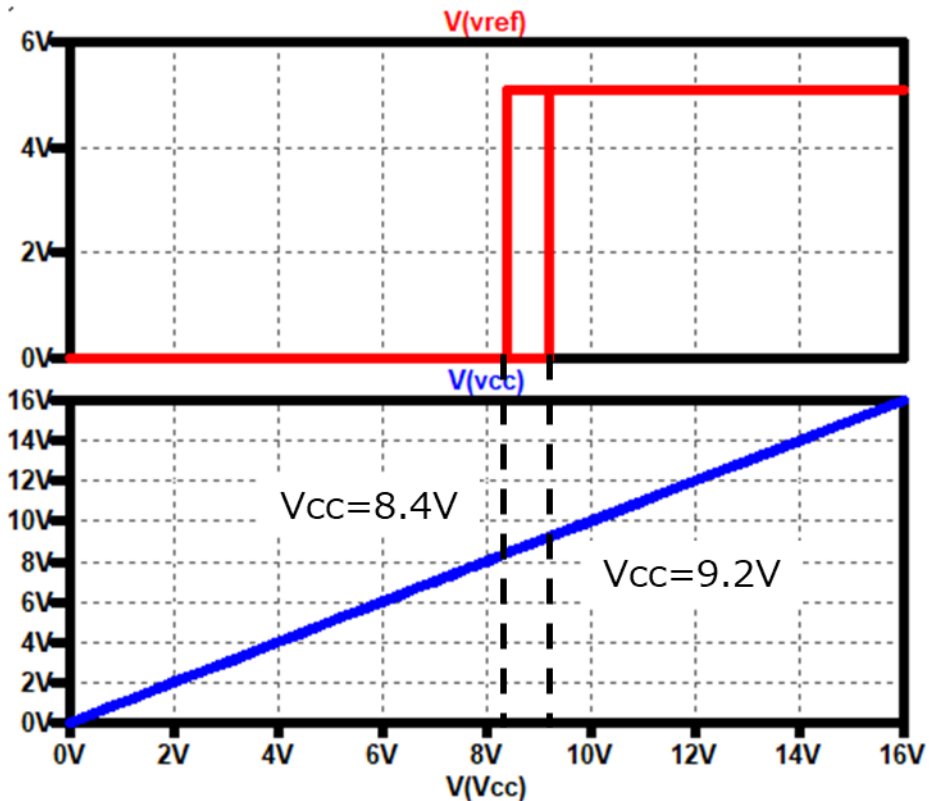
UVLO Testbench

Referred to Data Sheet



Simulation results are following.  
 Explanatory notes — : simulated

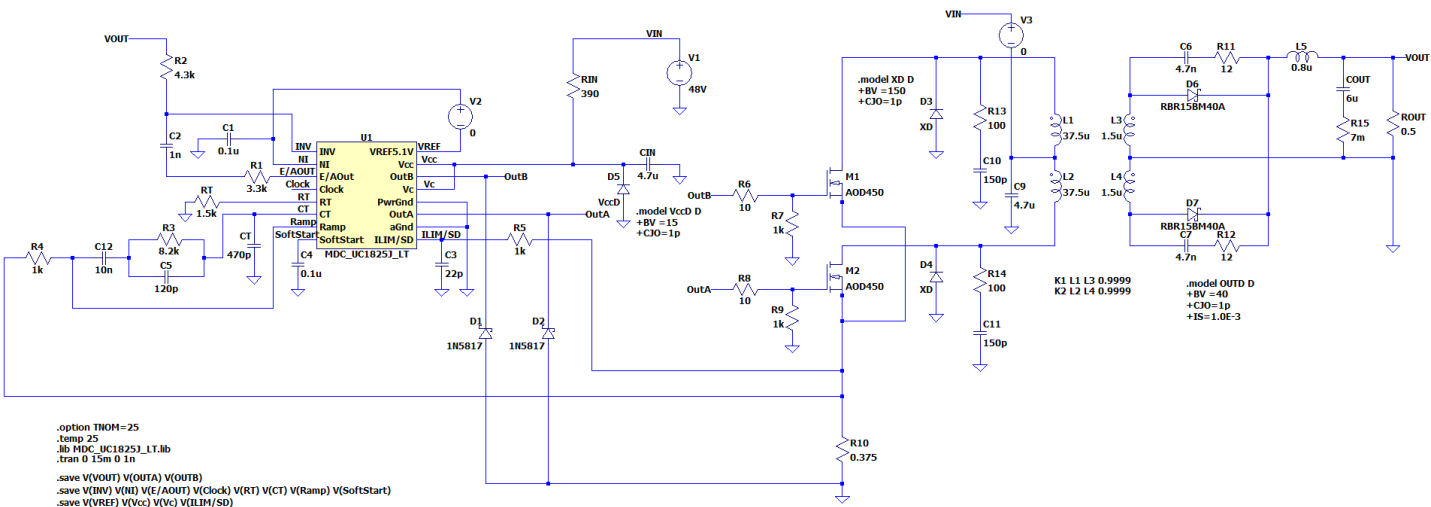
UVLO



V<sub>OUT</sub> Testbench

Referred to Data Sheet

V<sub>OUT</sub> :5.0V I<sub>OUT</sub> :10.0A



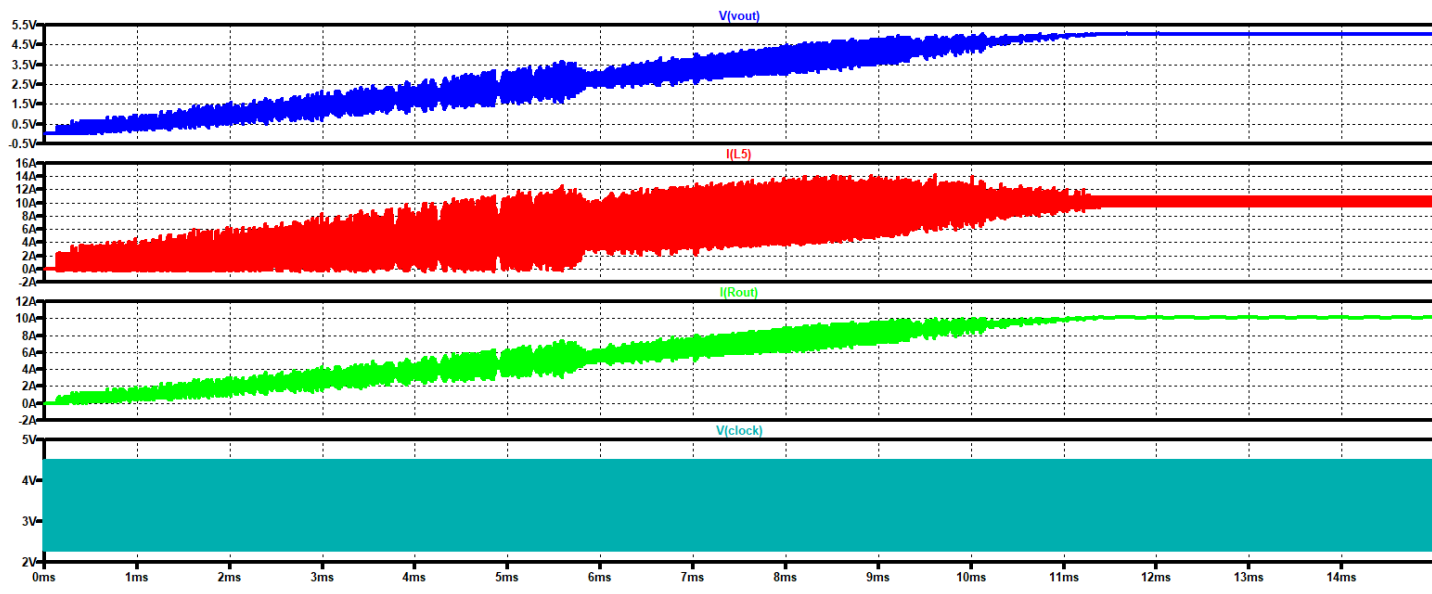
```

.option THOM=25
.temp 25
.lib MDC_UC1825J_LT.lib
.tran 0 15m 0 1n

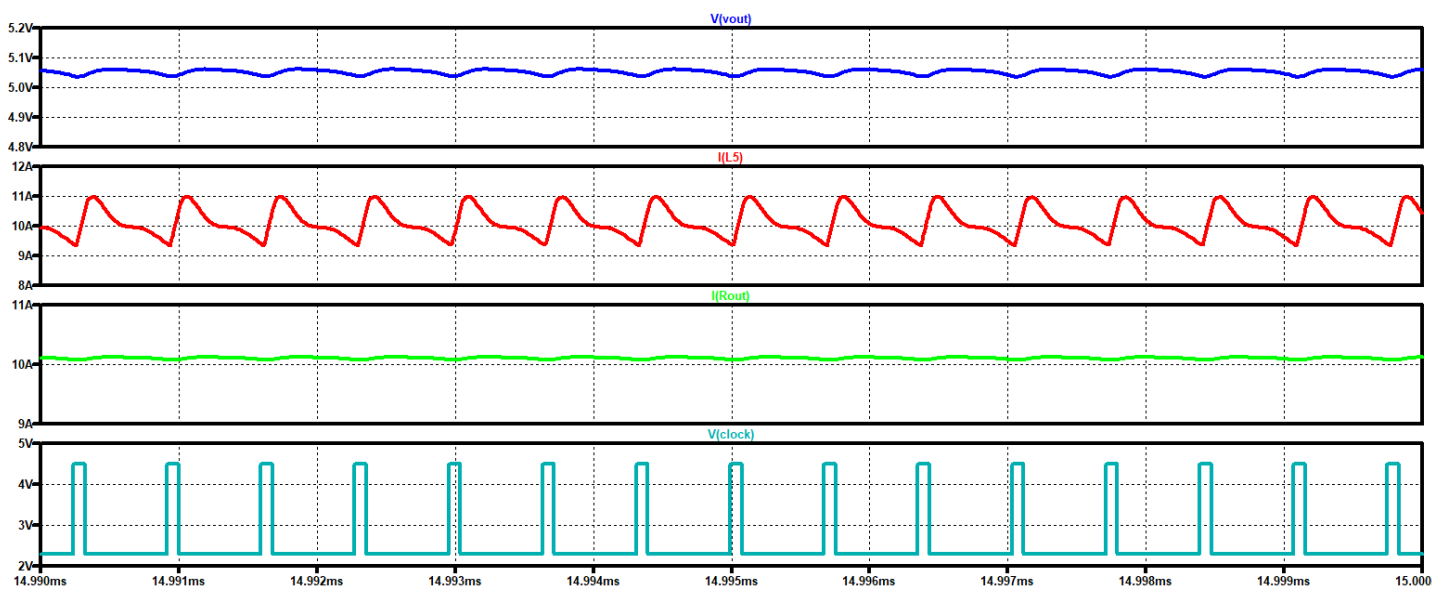
.save V(VOUT) V(OUTA) V(OUTB)
.save V(DIV) V(N1) V(E/AOUT) V(clock) V(RT) V(CT) V(Ramp) V(SoftStart)
.save V(VREF) V(Vcc) V(Vc) V(ILIM/SD)
.save I(I1) I(L2) I(L3) I(L4) Id(M1) Id(M2) I(COUT) I(ROUT) I(L5)
.save I(V3)
    
```

Simulation results are following.  
Explanatory notes — : simulated

**V<sub>OUT</sub> ( 0-15ms )**



**V<sub>OUT</sub> ( 14.99ms-15ms )**



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