

LTspice Model

NMOS

STM

STB45N65M5



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_STB45N65M5_LT
Pin Assign 1:D 2:G 3:S
File List Model Library MDC_STB45N65M5_LT01.lib
 Model Report MDC_STB45N65M5_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev 4
- Product name STB45N65M5
- Company name STMicroelectronics
- Characteristics IdVgs[Temp], IdVds[Vgs], Rds(on)Id[Vgs], Rds(on)Temp[Id], VthTemp[Id], Crss, Ciss, Coss, VgsQg[Vdd], VdsQg[Vdd], IsVsd[Temp], tdon, tdoff, tf, tr

Simulation Range

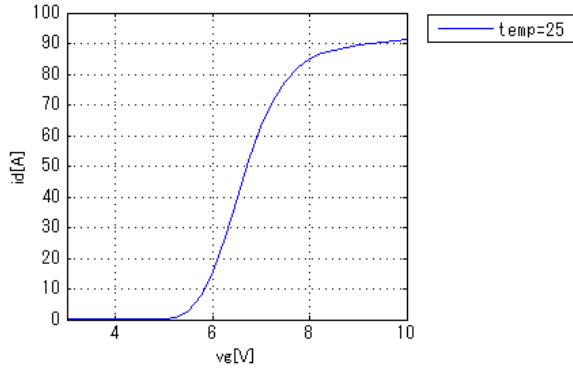
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	710	V
Gate-source voltage (DC)	0	to	25	V
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

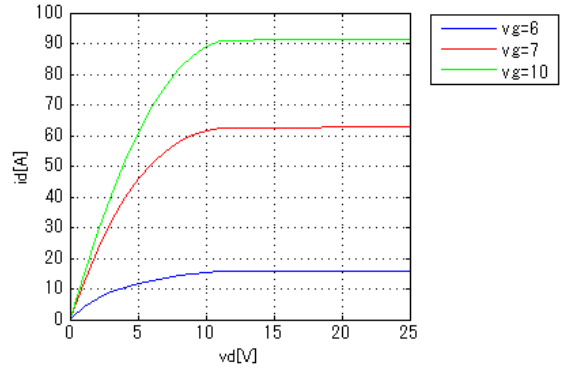
IdVgs[Temp]

Vds = 25V



IdVds[Vgs]

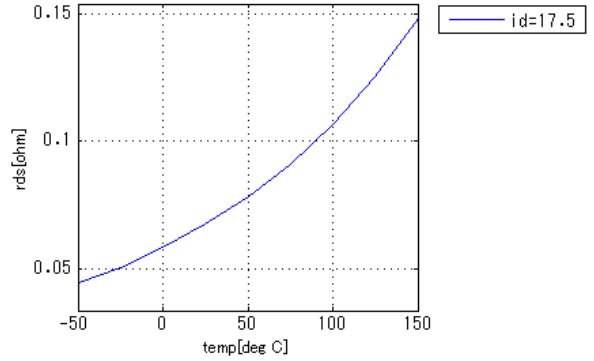
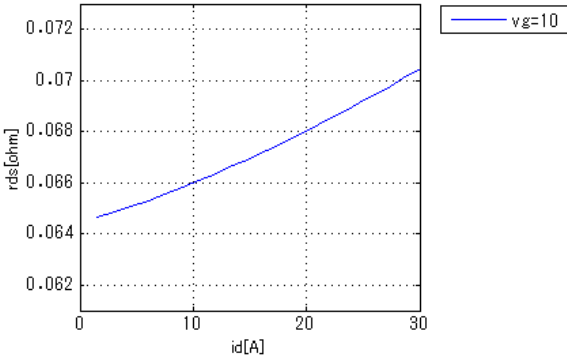
Temp. = 25deg C



Rds(on)Id[Vgs]

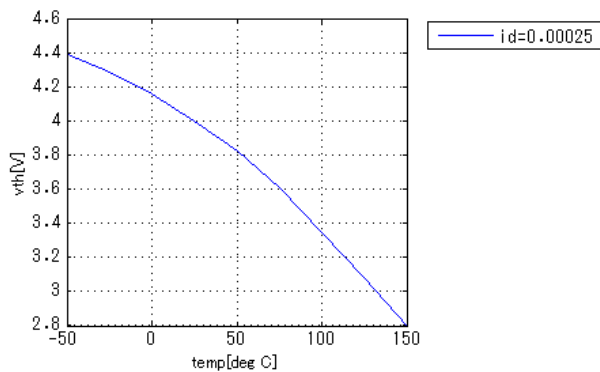
Rds(on)Temp[Id]

Vgs = 10V



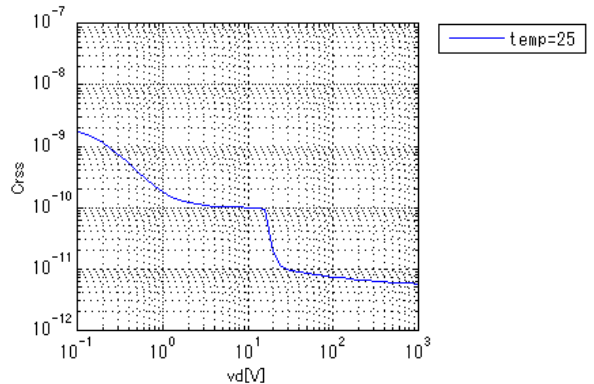
VthTemp[Id]

Vd = Vg



Crss

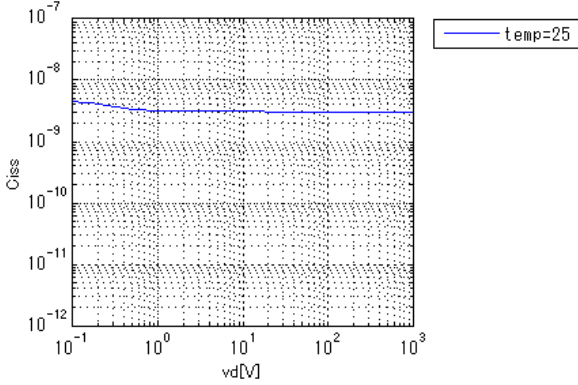
Freq. = 1MHz



Simulation results are following.
 Explanatory notes — : simulated

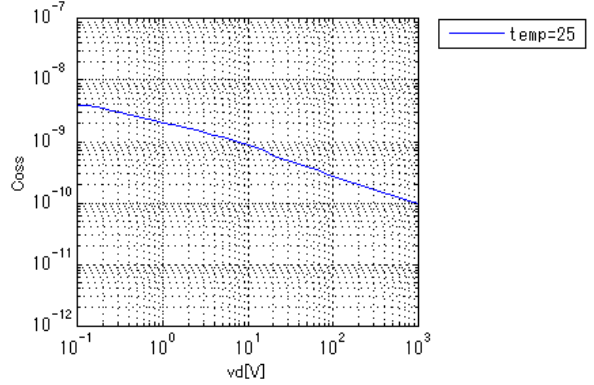
Ciss

Freq. = 1MHz



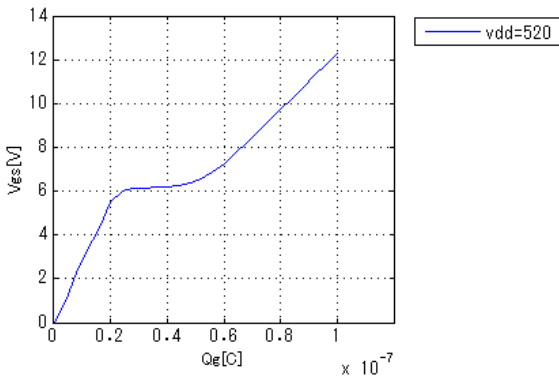
Coss

Freq. = 1MHz



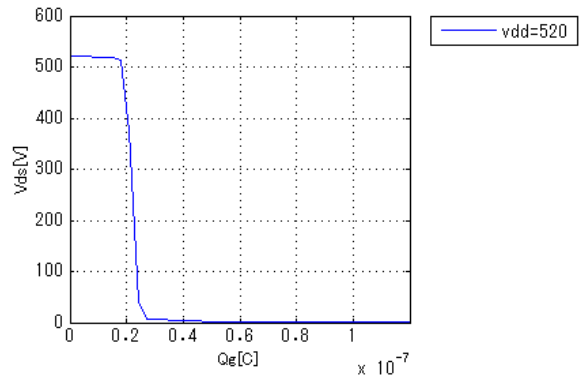
VgsQg[Vdd]

Id = 17.5A

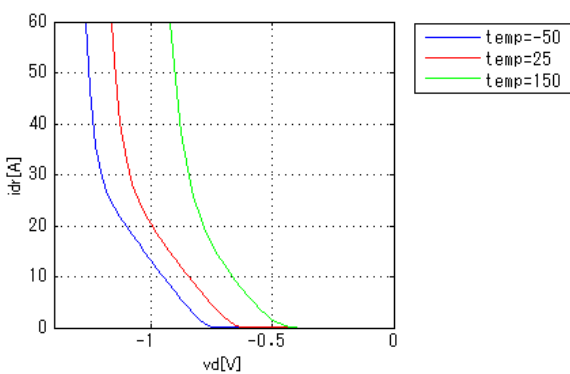


VdsQg[Vdd]

Id = 17.5A

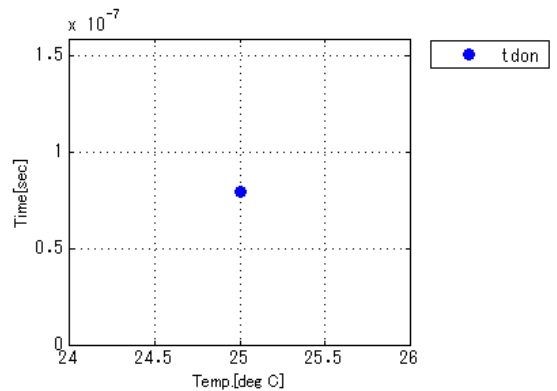


IsVsd[Temp]



tdon

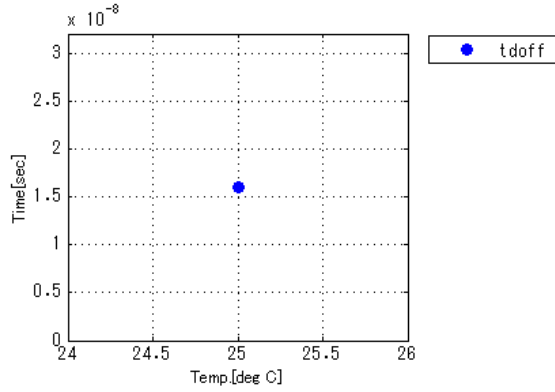
Vdd = 400V, Id = 23A, +Vg = 10V, -Vg = 0V, Rg = 0.001ohm



Simulation results are following.
 Explanatory notes — : simulated

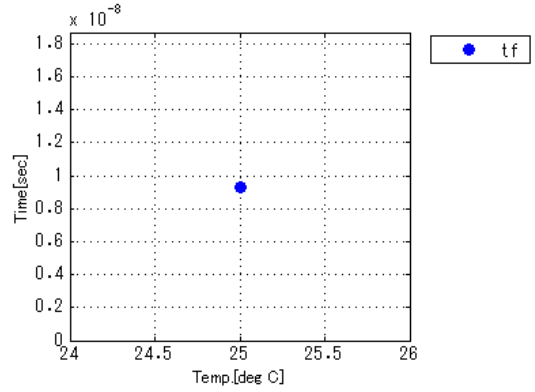
tdoff

Vdd = 400V, Id = 23A, +Vg = 10V, -Vg = 0V, Rg = 0.001ohm



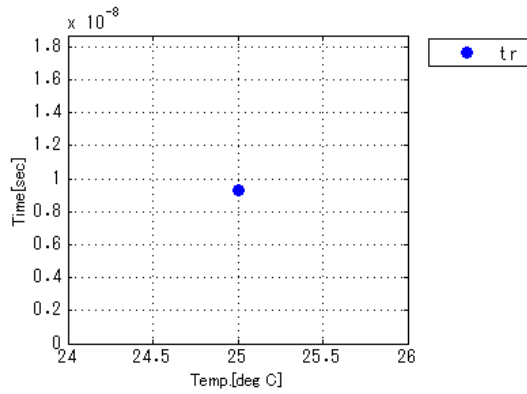
tf

Vdd = 400V, Id = 23A, +Vg = 10V, -Vg = 0V, Rg = 0.001ohm



tr

Vdd = 400V, Id = 23A, +Vg = 10V, -Vg = 0V, Rg = 0.001ohm



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