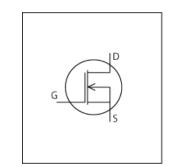


LTspice Model NMOS Infineon IPD60N10S4L-12



Model Information

Model A macro model based on BSIM3 model

Call Name MDC IPD60N10S4L-12 LT

Pin Assign 1:G 2:D 3:S

File List Model Library MDC_IPD60N10S4L-12_LT01.lib

Model Report MDC_IPD60N10S4L-12_LT.pdf (this file)

Verified Simulator Version

Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version
 Product name
 2011-11-30 Rev. 1.0
 IPD60N10S4L-12

■Company name Infineon Technologies AG

 $\begin{tabular}{l} \blacksquare Characteristics & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Temp[Id],Vtolorised & IdVds[Vgs],Rds(on)Temp[Id],Vto$

hTemp[Id],CapacitanceVds[Cname],IsVsd[Temp],BvTemp[ir],VgsQg[Vdd],SwitchingIdd[Tname],Trrlf[Ir],Qrrlf[Ir],Switching

Waveform, TrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	100	V
Gate-source voltage (DC)	-16	to	16	V
Temperature	-55	to	175	deg C



Model Functions Table

MOSFET

O: Implemented

× : Not Implemented
—: Not applicable

RANK=1

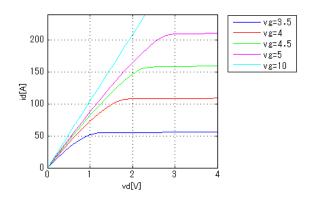
	KANK-1	
Functions	RANK	Implemented
ID-VDS-VGS	1	0
ID-VGS(Temp)	1	0
RDS(on)	1	0
Capacitance	1	0
Gate Charge	1	0
IS-VSD(Forward)	1	0
Reverse recovery	1	0
Switching(Typ.)	1	0
Bv	1	0
Yfs	1	_
Vth	1	0



Simulation results are following. Explanatory notes — : simulated

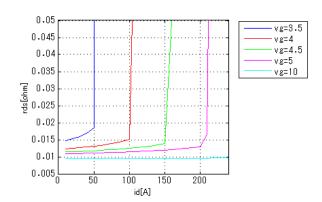
IdVds[Vgs]

Temp = 25degC



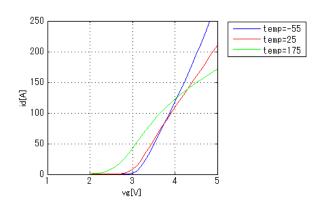
Rds(on)Id[Vgs]

Temp = 25degC



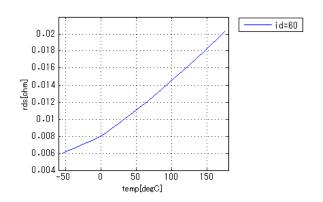
IdVgs[Temp]

Vds = 6V



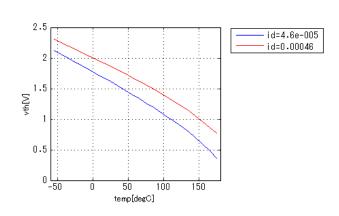
Rds(on)Temp[Id]

Vgs = 10V



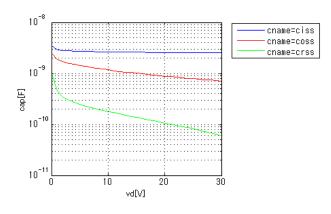
VthTemp[Id]

Vd = Vg



CapacitanceVds[Cname]

freq = 1000000Hz

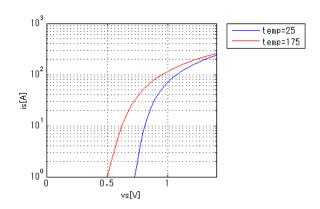




Simulation results are following. Explanatory notes — : simulated

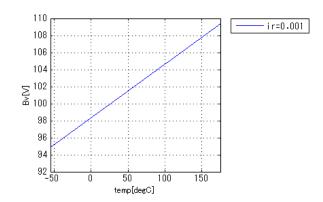
IsVsd[Temp]

vg = 0V



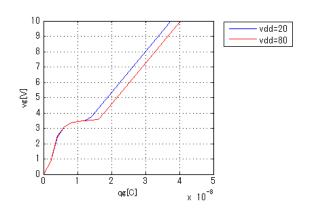
BvTemp[ir]

ir = 0.001A



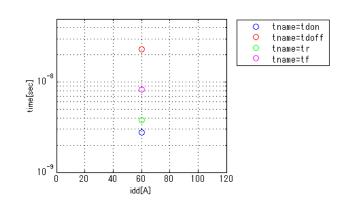
VgsQg[Vdd]

Id = 60A



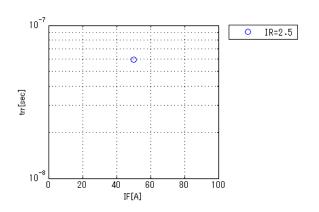
Switchingldd[Tname]

vgg = 10V, vdd = 50V, RGG = 3.50hm



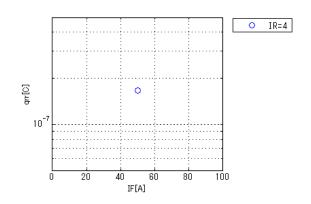
Trrlf[lr]

vdd = 50V, didt = 100A/us, Temp = 25degC



Qrrlf[lr]

vdd = 50V, didt = 100A/us, Temp = 25degC

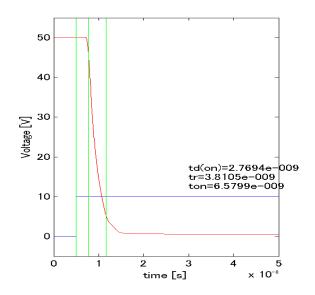


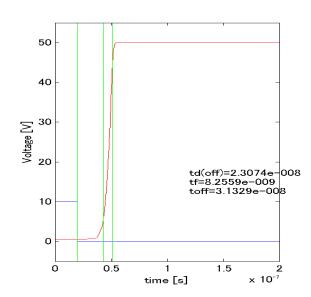


Simulation results are following. Explanatory notes — : simulated

Switching Waveform (Blue : INPUT Red : OUTPUT)

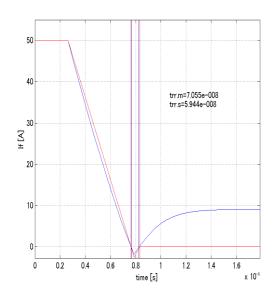
vgg = 10V, vdd = 50V, RGG = 3.5ohm, Temp = 25degC, Idd = 60A





Trr Waveform (Red: Datasheet Blue: Simulation)

didt = 100A/us, vcc = 10V, if = 50A, ir = 2.5A





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