

LTspice Model LDO (Low Drop Out) TOREX XC6701D502PR-G

Model Information

 Model
 An original macro model

 Call Name
 MDC_XC6701D502PR-G_LT

 Pin Assign
 1:VOUT 2:VSS 3:VIN

 File List
 Model Library
 MDC_XC6701D502PR-G_LT01.lib

 Model Report
 MDC_XC6701D502PR-G_LT.pdf (this file)

Verified Simulator Version Note

LTspice version XVII

References

The information which was used for modeling is as follow:

ETR0334-012b XC6701D502PR-G TOREX SEMICONDUCTOR LTD. Vdiflout[Temp],Line regulation,Load regulation

Simulation Condition

This table shows the value of evaluated simulation condition that was not occurs any convergence problems in this area.

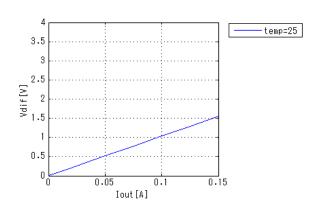
Item	Condition	Unit
Temperature	25	deg C



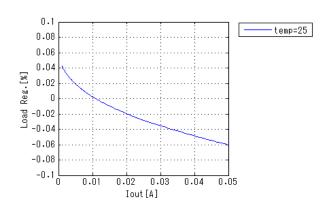
Simulation results are following. Explanatory notes — : simulated

Vdiflout[Temp]

Temp. = 25deg C

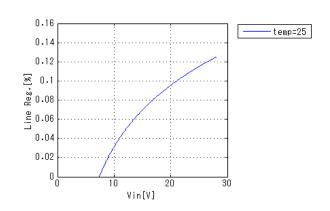


Load regulation



Line regulation

lout = 13mA





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