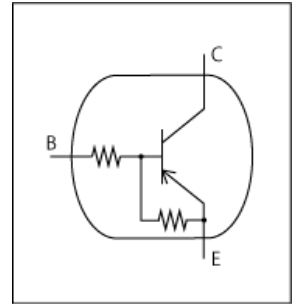


LTspice Model

BRT (Bias Resistor Transistor)

KEC

KRA305



Model Information

Model A macro model based on Gummel-Poon model
Call Name MDC_KRA305_LT
Pin Assign 1:C 2:B 3:E
File List Model Library MDC_KRA305_LT02.lib
 Model Report MDC_KRA305_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Revision No : 5
- Product name KRA305
- Company name KEC Corporation
- Characteristics IcVi[OFF],IcVi[ON],hFEIc[Temp]

Simulation Range

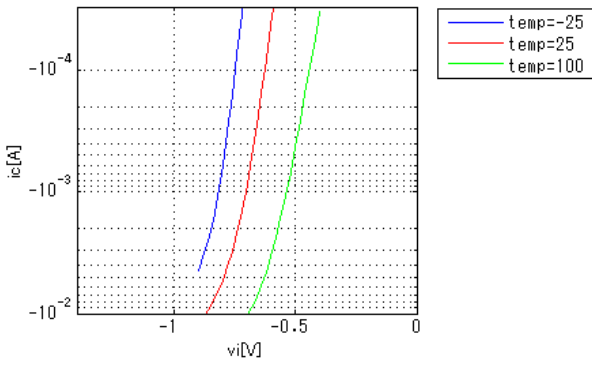
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	-50	V
Base current (DC)	0	to	-3.6m	A
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

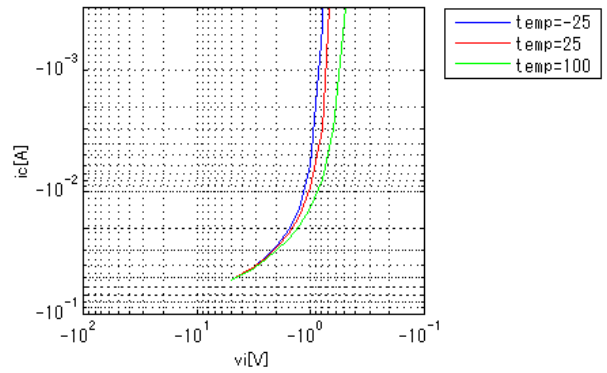
IcVi[OFF]

Vce = -5V



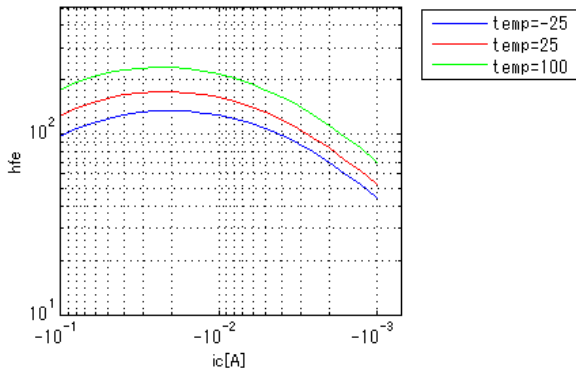
IcVi[ON]

Vce = -0.2V



hFEIc[Temp]

Vce = -5V



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