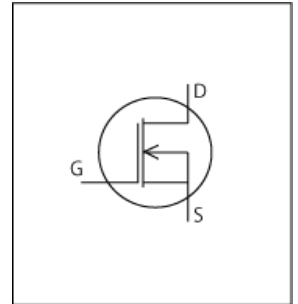


PSpice Model

NMOS

STM

STL210N4F7AG



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_STL210N4F7AG_PS
Pin Assign 1:S 2:S 3:S 4:G 5:D 6:D 7:D 8:D
File List Model Library MDC_STL210N4F7AG_PS01.lib
 Model Report MDC_STL210N4F7AG_PS.pdf (this file)

Verified Simulator Version PSpice version 17.2
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version January 2016 Rev 1
- Product name STL210N4F7AG
- Company name STMicroelectronics N.V.
- Characteristics IdVds[Vgs], IdVgs[Temp], VgsQg[Vdd], Rds(on)Id[Vgs], CapacitanceVds[Cname], Rds(on)Temp[Vgs], BvTemp[Ir], VthTemp[Id], VsdIs[Temp], SwitchingIdd[Tname], SwitchingWaveform, Trrrf[Ir], Qrrf[Ir], TrrQrrWaveform

Simulation Range

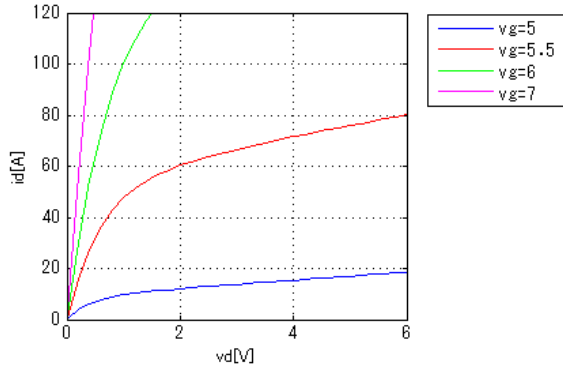
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C

Simulation results are following.
 Explanatory notes — : simulated

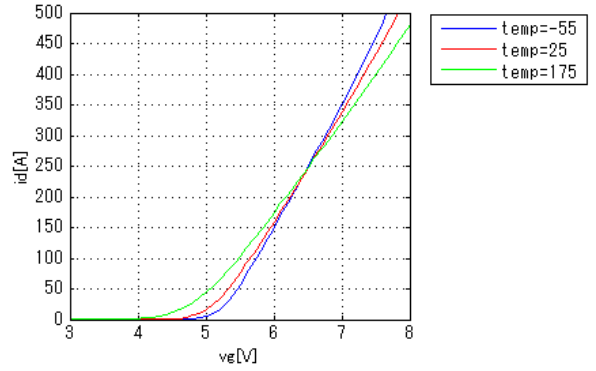
IdVds[Vgs]

Temp. = 25degC



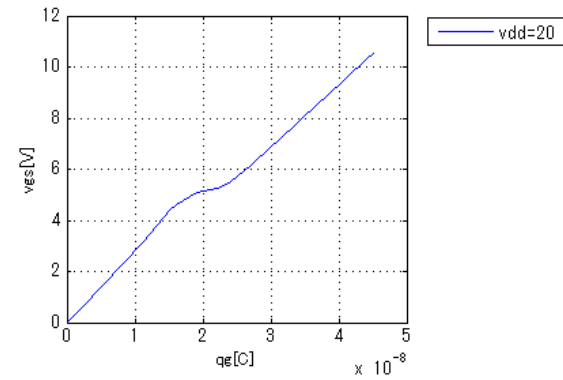
IdVgs[Temp]

Vds = 5V

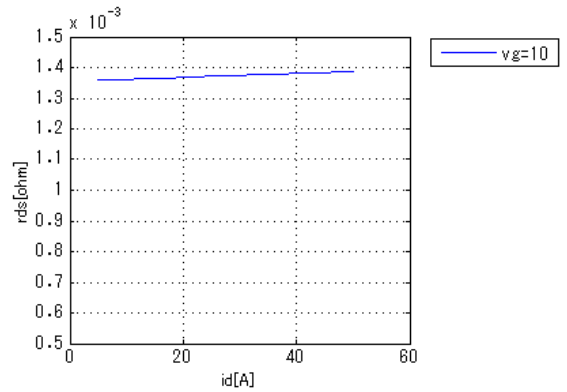


VgsQg[Vdd]

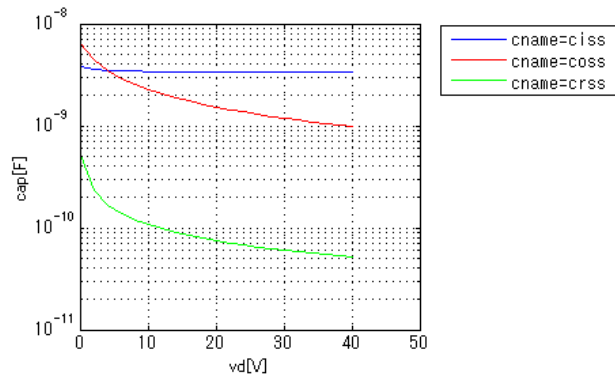
Id = 40A



Rds(on)Id[Vgs]

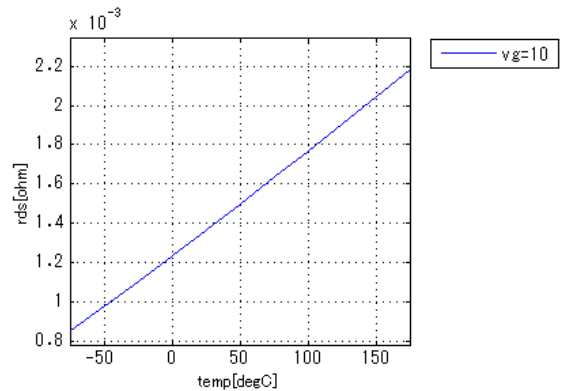


CapacitanceVds[Cname]



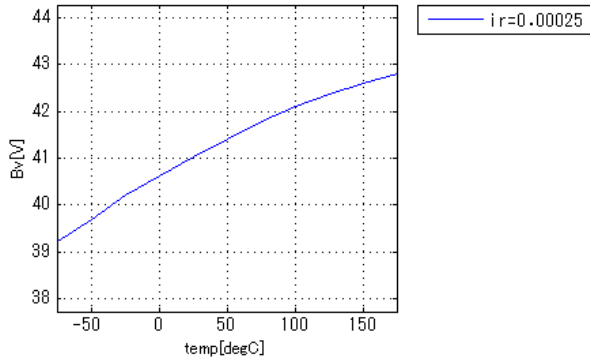
Rds(on)Temp[Vgs]

Id = 16A



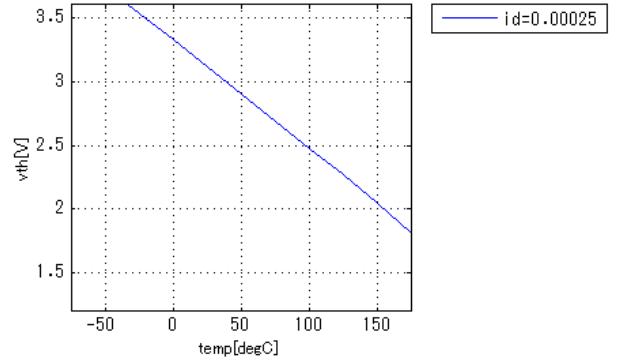
Simulation results are following.
 Explanatory notes — : simulated

BvTemp[Ir]

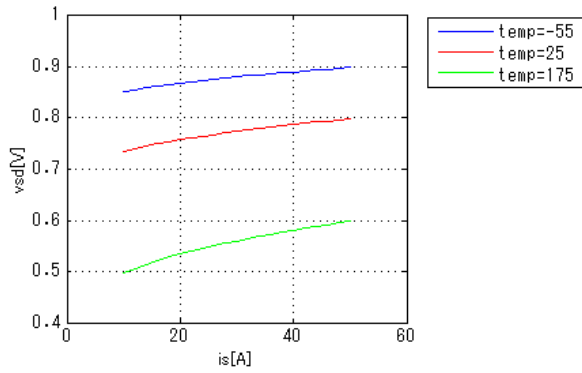


VthTemp[Id]

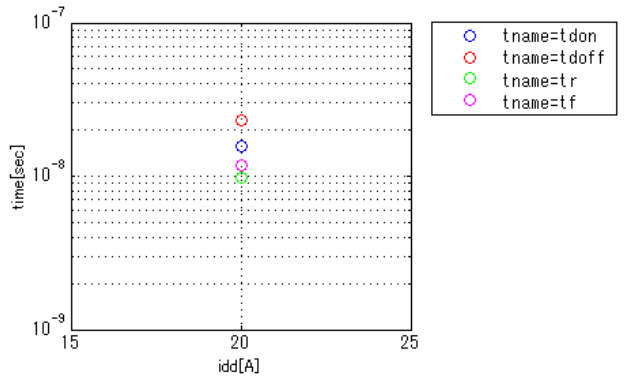
Vd = Vg



VsdIs[Temp]

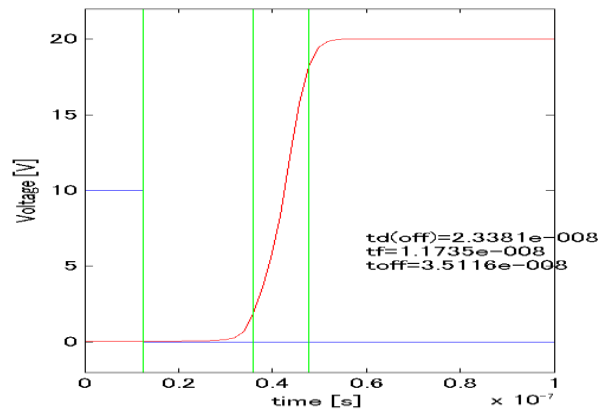
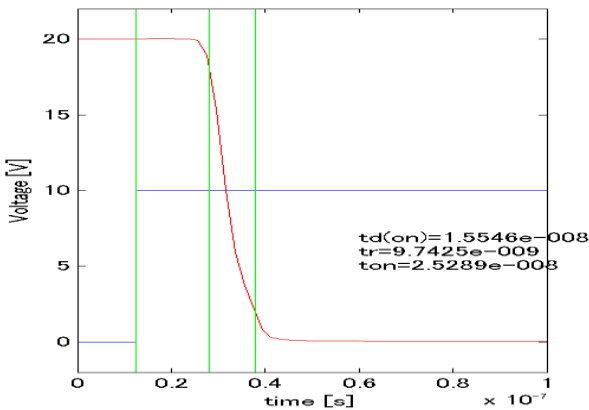


SwitchingIdd[Tname]



SwitchingWaveform

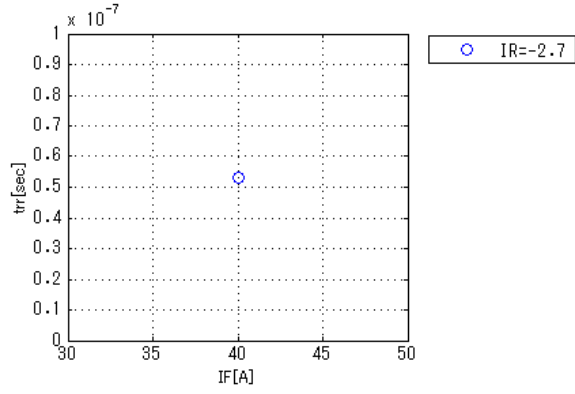
Blue : INPUT Red : OUTPUT



Simulation results are following.
 Explanatory notes — : simulated

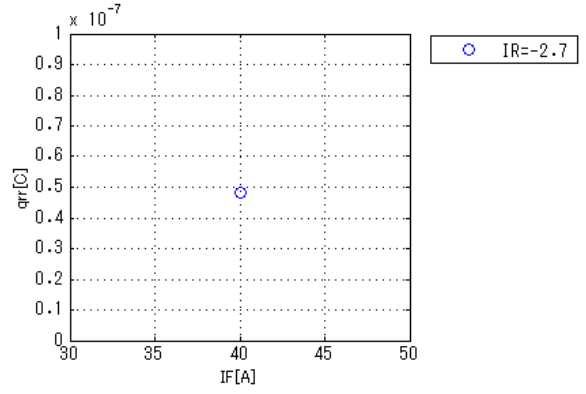
Trrlf[I_r]

didt = 100A/us



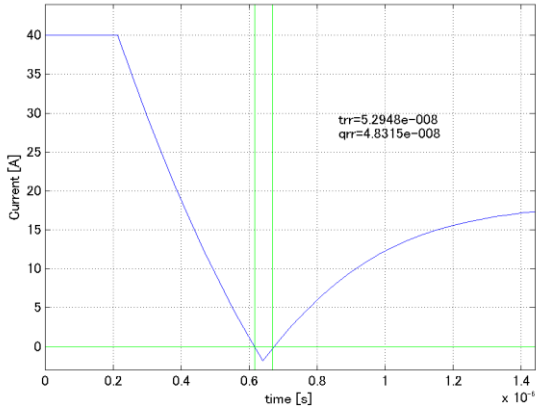
Qrrlf[I_r]

didt = 100A/us



TrrQrrWaveform

didt = 100A/us



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