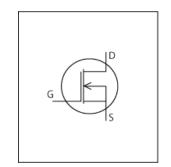


# LTspice Model NMOS TI CSD17313Q2



# **Model Information**

Model A macro model based on BSIM3 model

Call Name MDC\_CSD17313Q2\_LT Pin Assign 1:D 2:D 3:G 4:S 5:D 6:D

File List Model Library MDC\_CSD17313Q2\_LT01.lib

Model Report MDC\_CSD17313Q2\_LT.pdf (this file)

**Verified Simulator Version** 

Note

LTspice version XVII

#### References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version REVISED SEPTEMBER 2015

Product name CSD17313Q2

●Company name Texas Instruments Inc.

● Characteristics IdVds[Vgs],IdVgs[Temp],VgsQg[Vdd],CapacitanceVds[Cnam

e],VthTemp[Id],Rds(on)Vgs[Temp],Rds(on)Temp[Vgs],Rds(on)Temp[Vgs]02,IsVsd[Temp],SwitchingIdd[Tname],Switching

Waveform, Trrlf[Ir], Qrrlf[Ir], TrrQrrWaveform

#### Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

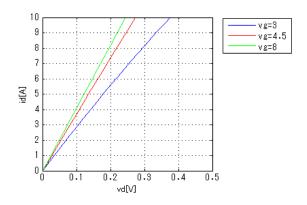
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	30	V
Gate-source voltage (DC)	-8	to	10	V
Temperature	-55	to	150	deg C



Simulation results are following. Explanatory notes — : simulated

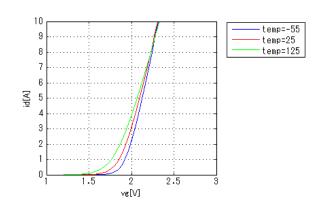
# IdVds[Vgs]

Temp. = 25degC



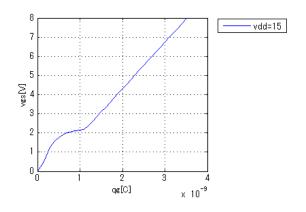
# IdVgs[Temp]

Vds = 5V



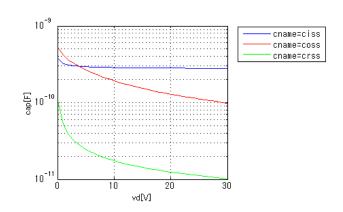
# VgsQg[Vdd]

Id = 4A



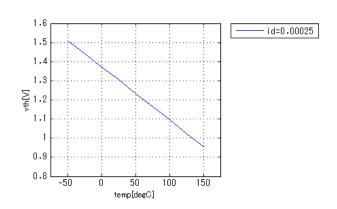
# CapacitanceVds[Cname]

freq = 1000000Hz



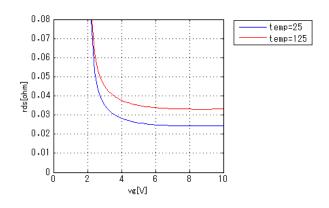
#### VthTemp[Id]

Vd = Vg



# Rds(on)Vgs[Temp]

Id = 4A

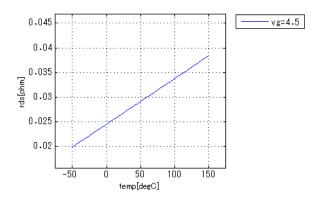




Simulation results are following. Explanatory notes — : simulated

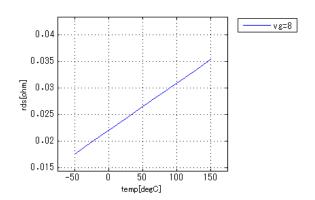
# Rds(on)Temp[Vgs]

Id = 4A

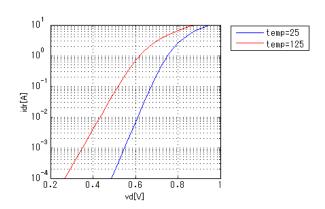


# Rds(on)Temp[Vgs]02

Id = 4A

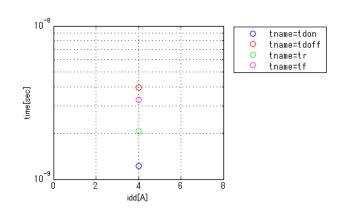


# IsVsd[Temp]



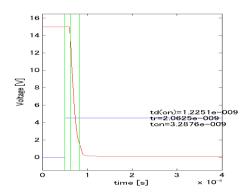
### SwitchingIdd[Tname]

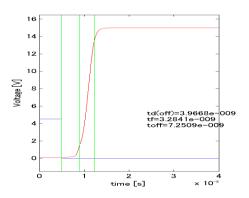
vgg = 4.5V, vdd = 15V, RGG = 2.0ohm



#### **SwitchingWaveform**

Blue: INPUT Red: OUTPUT



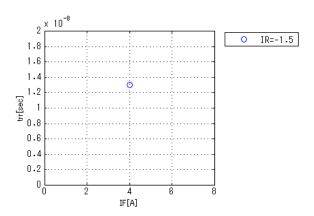




Simulation results are following. Explanatory notes — : simulated

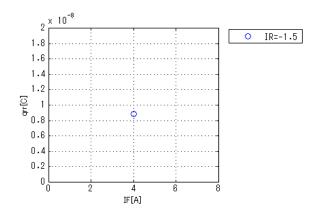
# Trrlf[lr]

vdd = 13.5V, didt = 300A/us

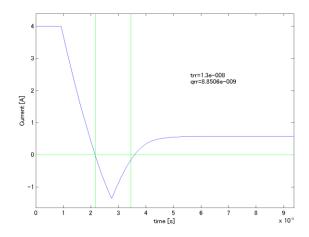


# Qrrlf[lr]

vdd = 13.5V, didt = 300A/us



#### **TrrQrrWaveform**





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MoDeCH Inc.

**Head Office** 

Location: Taiju-Seimei-Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan

Tel:+81-42-656-3360

E-Mail:model-on-support@modech.co.jp

URL:http://www.modech.com/en/