

# LTspice Model **MOSFET Drive Switching Regulator IC** Nisshinbo Micro Devices Inc. NJW4140-Z2

#### **Model Information**

Model A macro model

**Call Name** MDC\_NJW4140-Z2\_LT

1:V+ 2:EN 3:IN- 4:FB 5:CT 6:GND 7:SI 8:OUT Pin Assign File List Model Library MDC\_NJW4140-Z2\_LT01.lib

Model Report MDC\_NJW4040-Z2\_LT.pdf(this file)

**Verified Simulator Version** LTspice 17.1.8

Note

#### References

The information which was used for modeling is as follow:

[Data Sheet]

Ver. 1.1 Date/Version Product name NJW4140-Z2

Company name Nisshinbo Micro Devices Inc.

[Characteristics listed]

Characteristics Fosc1, Vosc, Fdiv, Fosc\_low, Tss, Vb, Av, Gb Fosc1, Vosc, fdiv, fos lom+, lom-, Vt\_0, Vt\_50, Vipk, Tdelay, Roh, Rol

Ioh, Volim, Vt\_on, Vt\_off, Von, Voff Rpd, Idd\_stb

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition			Unit
	Min	Тур	Max	Offic
Supply Voltage	3.0		40.0	
Temperature		25.0		deg C



**Model Functions Table** 

# **Switching Regulator**

O:Implemented

×: Not Implemented

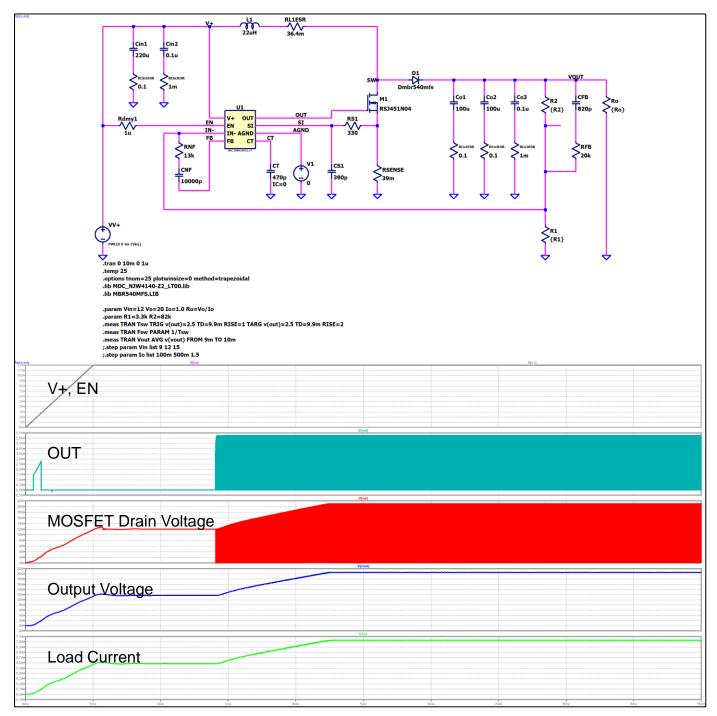
—: Not applicable

## RANK=1

	IVAIVIN-1	
Functions	RANK	Implemented
PWM Control	1	0
Wide Oscillating Frequency	1	0
Standby Function	1	0
Soft Start	1	0
Line Regulation	1	0
Load Regulation	1	0
UVLO	1	0
Over Current Protection	1	0

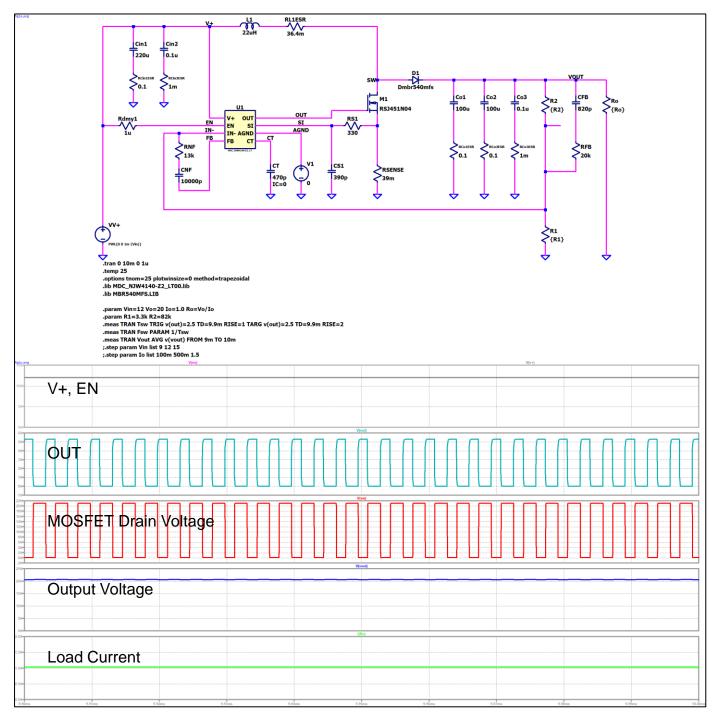


Testbench for PWM control (V = 12[V], Vout = 20[V], Iout = 1.5[A])



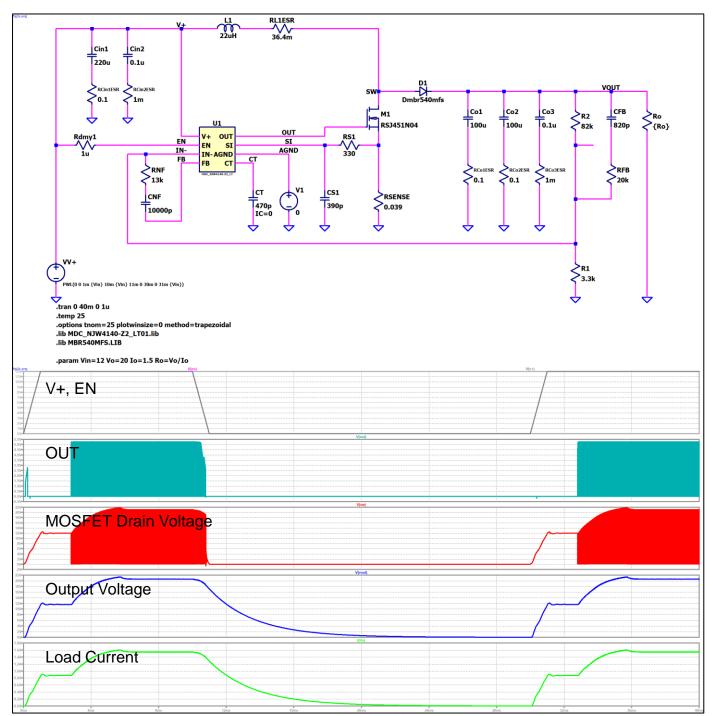


Testbench for PWM control (V+ = 12[V], Vout = 20[V], lout = 1.5[A]) [Extended view]



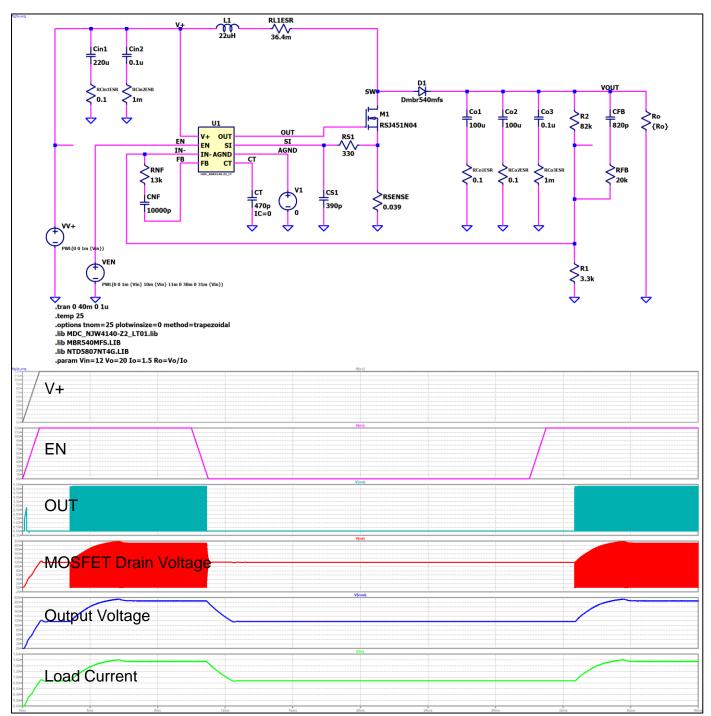


Testbench for UVLO function (V+ = 12[V], Vout = 20[V], lout = 1.5[A])



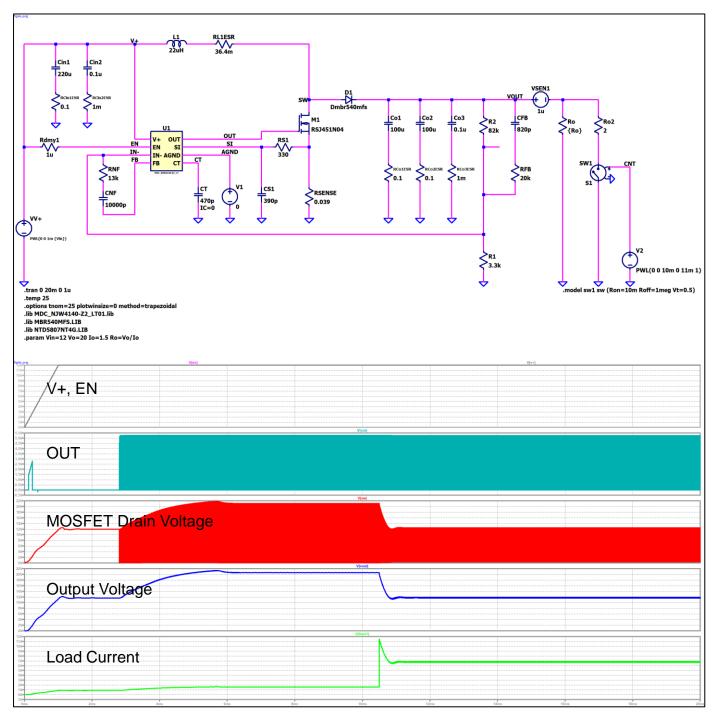


Testbench for EN function (V+ = 12[V], Vout = 20[V], Iout = 1.5[A])





Testbench for OPC function (V+ = 12[V], Vout = 20[V], lout =  $1.5[A] \rightarrow 10.0[A]$ )





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