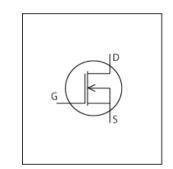


PSpice Model NMOS Infineon IAUC60N04S6N031H



Model Information

Model A macro model based on BSIM3 model

Call Name MDC IAUC60N04S6N031H PS

Pin Assign 1:G1 2:S1/D2 3:S1/D2 4:G2 5:S2 6:S2 7:D1 8:D1

File List Model Library MDC_IAUC60N04S6N031H_PS01.lib

Model Report MDC_IAUC60N04S6N031H_PS.pdf (this file)

Verified Simulator Version

Note

PSpice version 17.2

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version
Product name
Company name
Rev. 1.0 2020-09-22
IAUC60N04S6N031H
Infineon Technologies AG

● Characteristics IdVds[Vgs],Rds(on)Id[Vgs],IdVgs[Temp],Rds(on)Temp[Id],Vt

hTemp[Id],CapacitanceVds[Cname],IsVsd[Temp],BvTemp[ir],VgsQg[Vdd],SwitchingIdd[Tname],Trrlf[Ir],Qrrlf[Ir],Switching

Waveform, TrrQrrWaveform

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

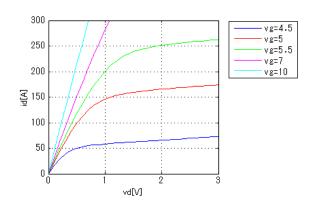
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	40	V
Gate-source voltage (DC)	-20	to	20	V
Temperature	-55	to	175	deg C



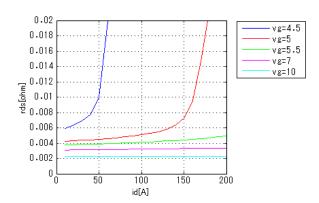
Simulation results are following. Explanatory notes — : simulated

IdVds[Vgs]

Temp. = 25degC

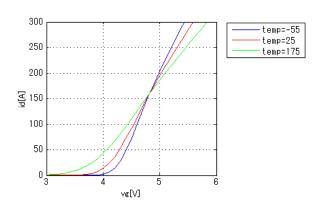


Rds(on)Id[Vgs]



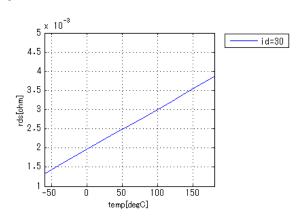
IdVgs[Temp]

Vds = 6V



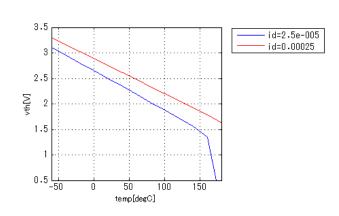
Rds(on)Temp[Id]

Vgs = 10V



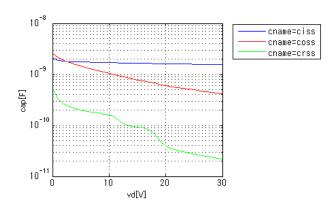
VthTemp[Id]

Vd = Vg



CapacitanceVds[Cname]

freq = 1000000Hz

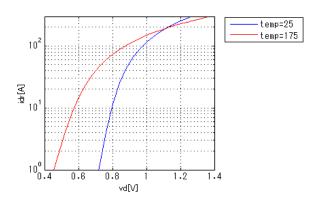




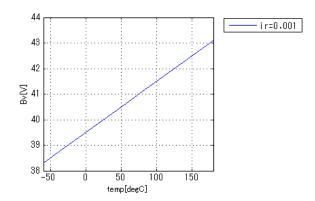
Simulation results are following. Explanatory notes — : simulated

IsVsd[Temp]

vg = 0V

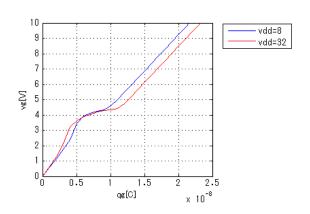


BvTemp[ir]



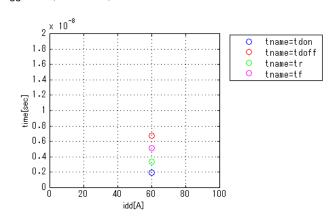
VgsQg[Vdd]

Id = 40A



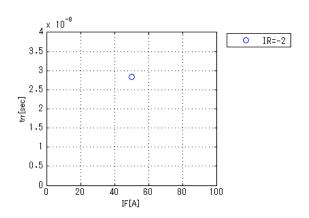
Switchingldd[Tname]

vgg = 10V, vdd = 20V, RGG = 3.50hm



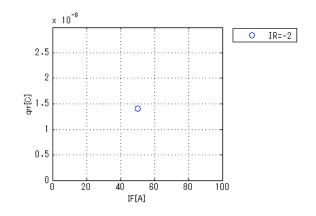
Trrlf[lr]

vdd = 20V, didt = 100A/us



Qrrlf[lr]

vdd = 20V, didt = 100A/us

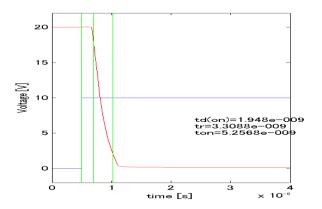


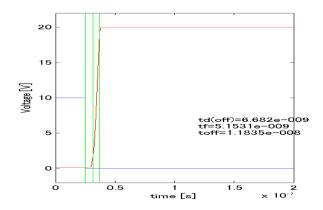


Simulation results are following. Explanatory notes — : simulated

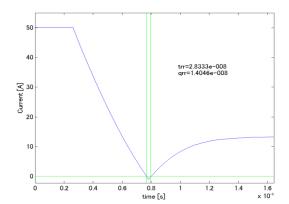
SwitchingWaveform

Blue: INPUT Red: OUTPUT





TrrQrrWaveform





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