

# PSpice Model

## Low Side Driver

### STMicroelectronics

### VNL5090S5-E

#### Model Information

**Model** A macro model  
**Call Name** MDC\_VNL5090S5-E\_PS  
**Pin Assign** 1:SUPPLY\_VOLTAGE 2: INPUT 3:STATUS 4:N.C 5:DRAIN1  
 6:SOURCE1 7:SOURCE2 8:DRAIN2  
**File List** Model Library MDC\_VNL5090S5-E\_PS01.lib  
 Model Report MDC\_VNL5090S5-E\_PS.pdf (this file)  
**Verified Simulator Version** OrCAD Ver17.2  
**Note**

#### References

The information which was used for modeling is as follow:

- [Data Sheet]
  - Date/Version November 2018 / DS8791 Rev 8
  - Product name VNL5090S5-E
  - Company name STMicroelectronics
- [Characteristics listed]
  - Characteristics
    - Current limitation
    - Under voltage
    - Open load detection
    - Overvoltage clamp protection
    - Input Clamp
    - Supply Clamp
    - Status Clamp

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

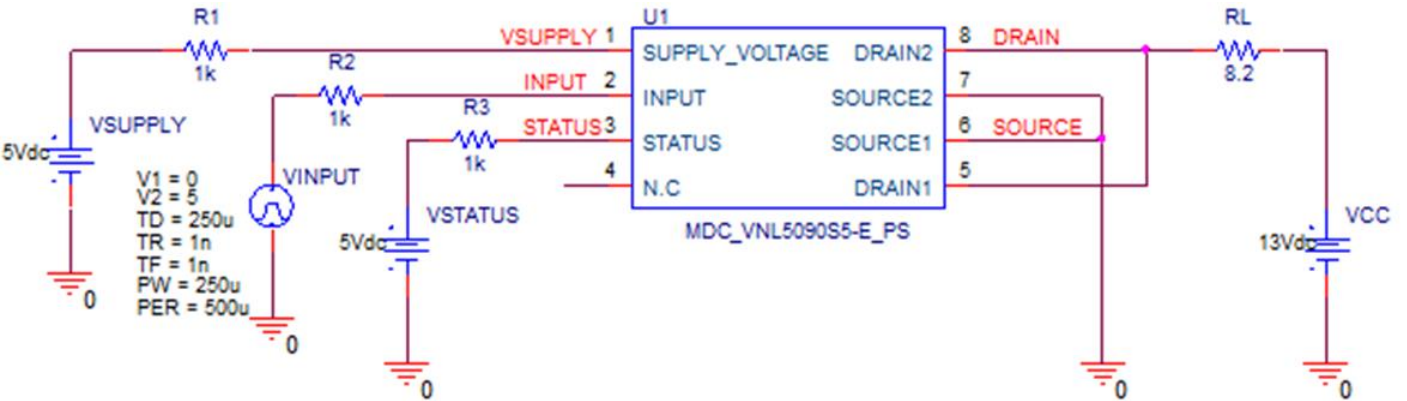
**Driver, IPD**

○ : Implemented  
 × : Not Implemented  
 – : Not applicable

**Model Functions Table**
**RANK=2**

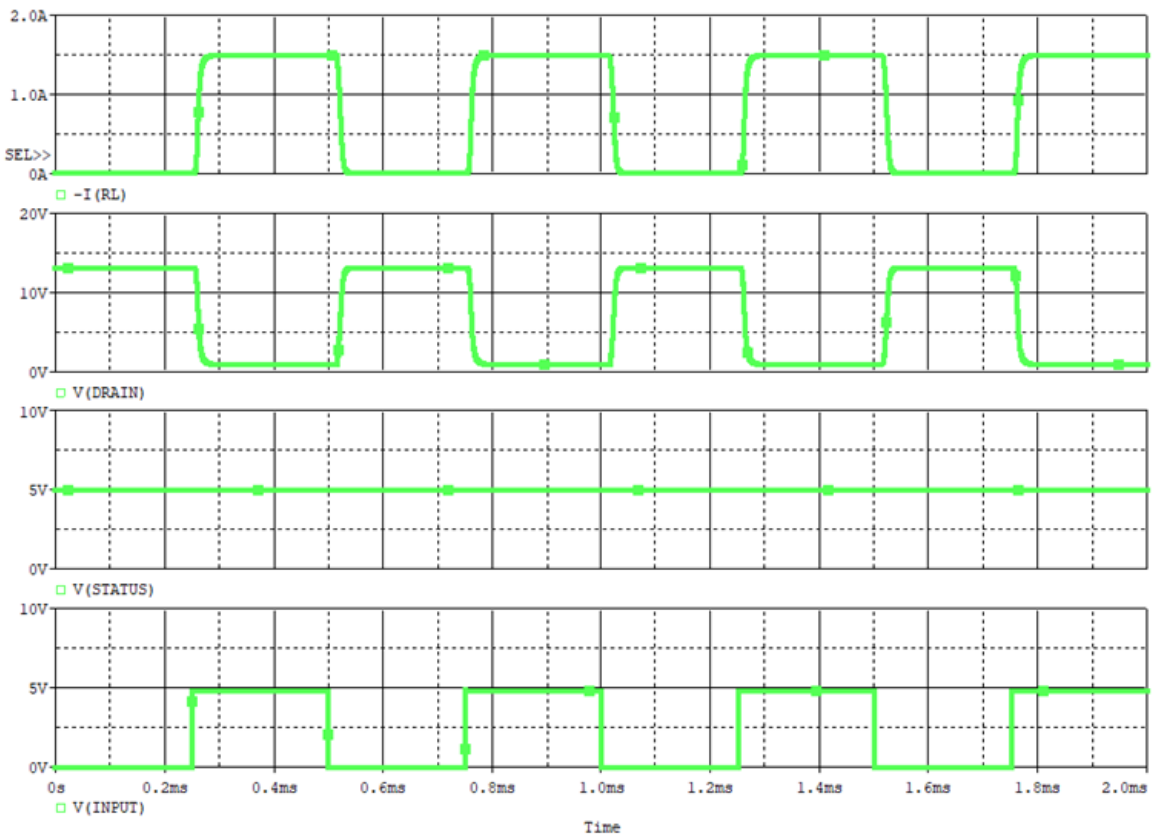
Functions	RANK	Implemented
Truth Table	1	○
On Resistance	1	○
Switching(Typ.)	1	○
UVLO	1	–
VH/VIL-VDD	1	–
Clamp Voltage	1	○
Propagation delay	1	–
Over Current Protection	2	○
Over Voltage Protection	2	–

Normal operation Testbench



Simulation results are following.  
 Explanatory notes — : simulated

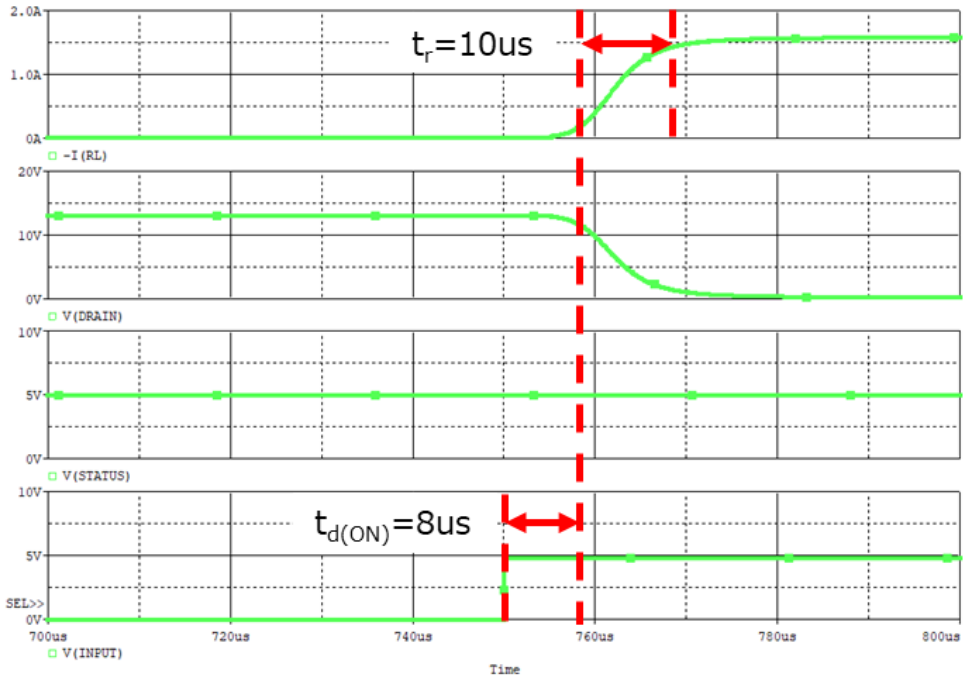
Normal operation



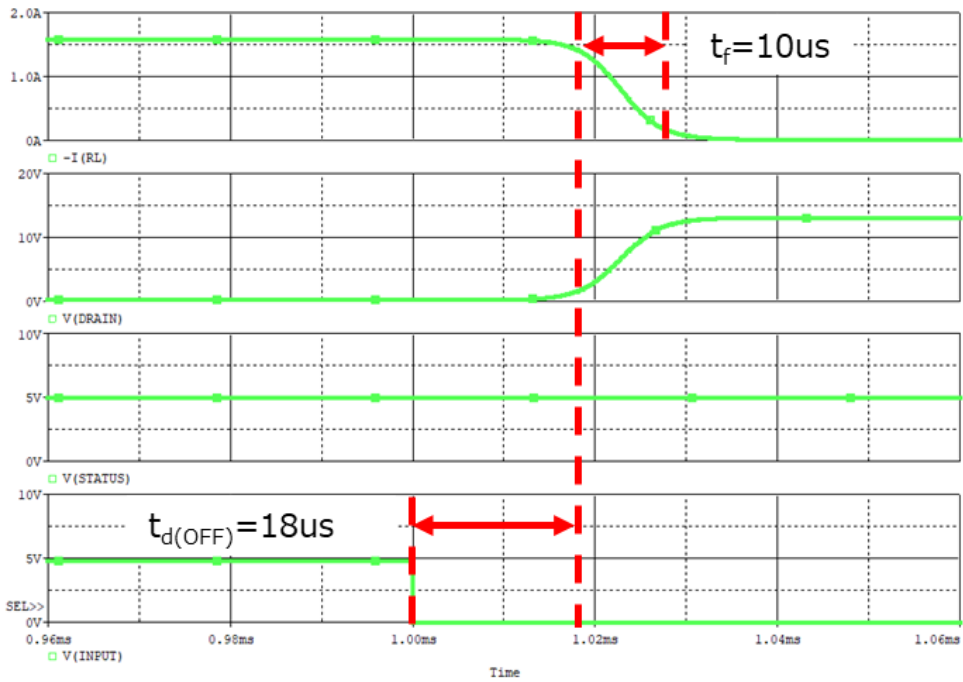
Simulation results are following.  
 Explanatory notes — : simulated

**Normal operation**

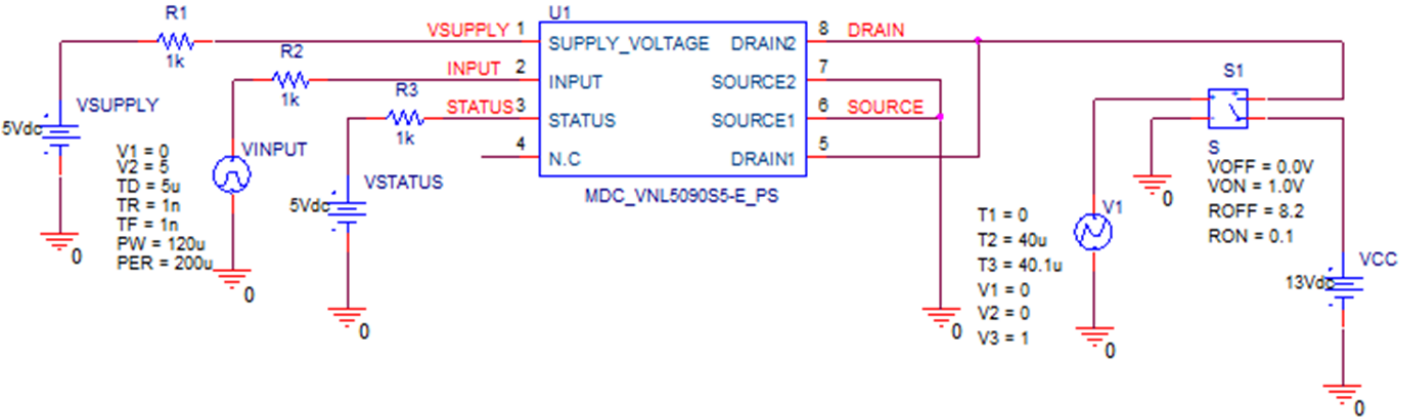
**$t_{d(ON)}, t_r$**



**$t_{d(OFF)}, t_f$**

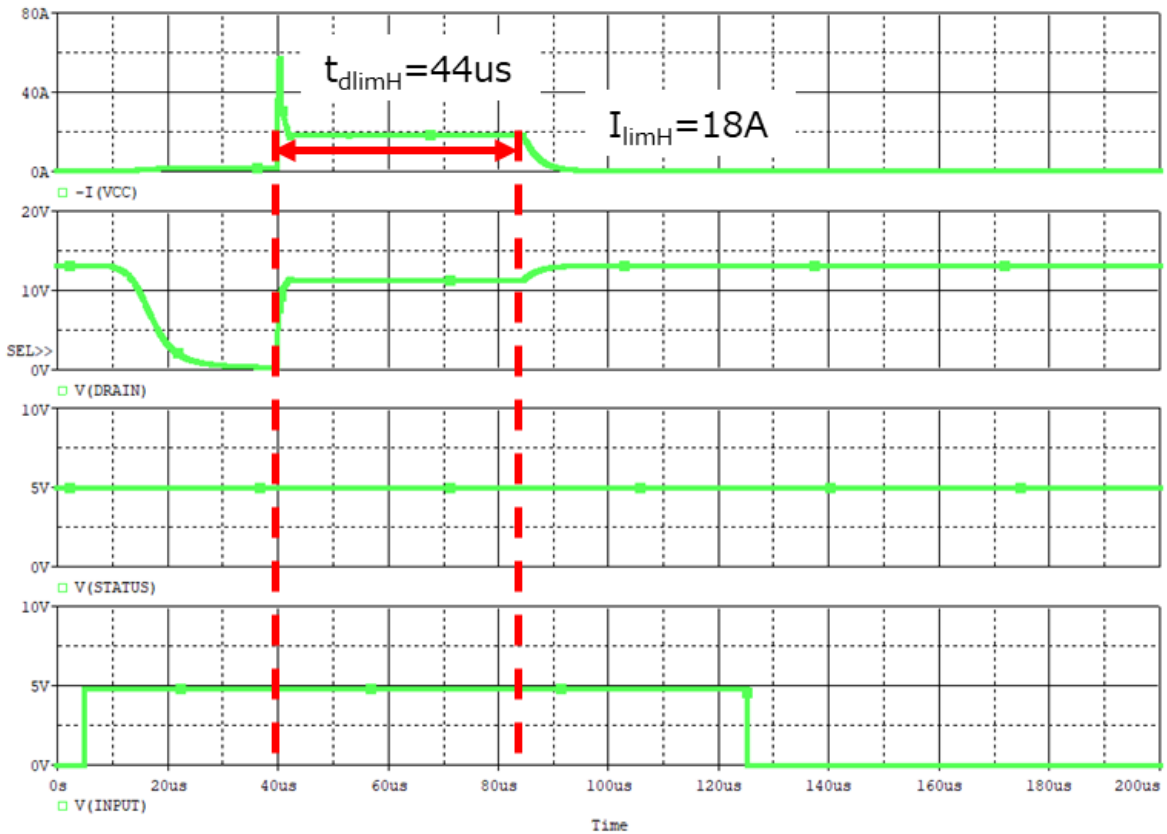


Current limitation Testbench

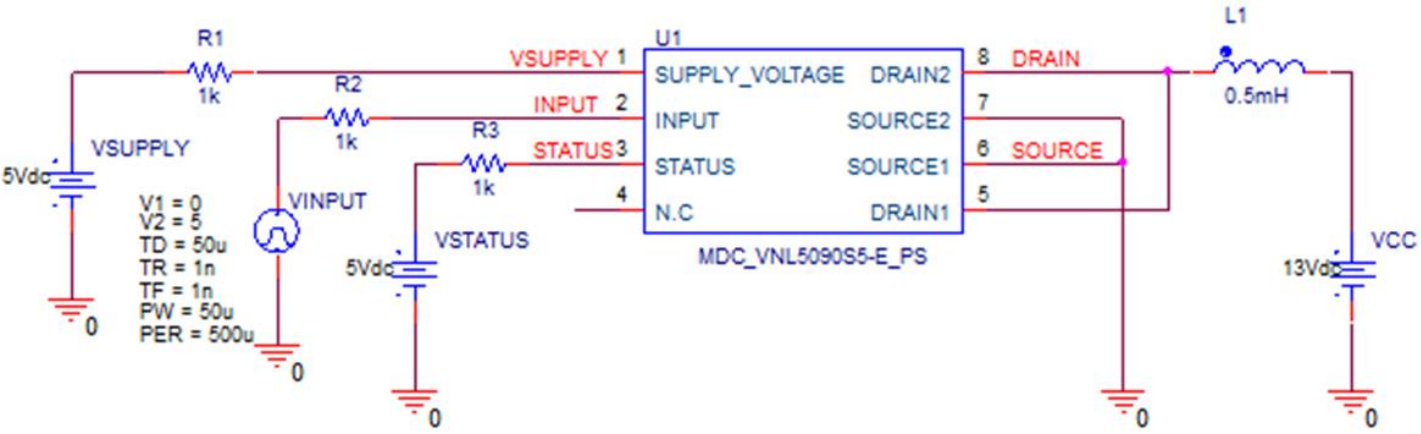


Simulation results are following.  
 Explanatory notes — : simulated

Current limitation

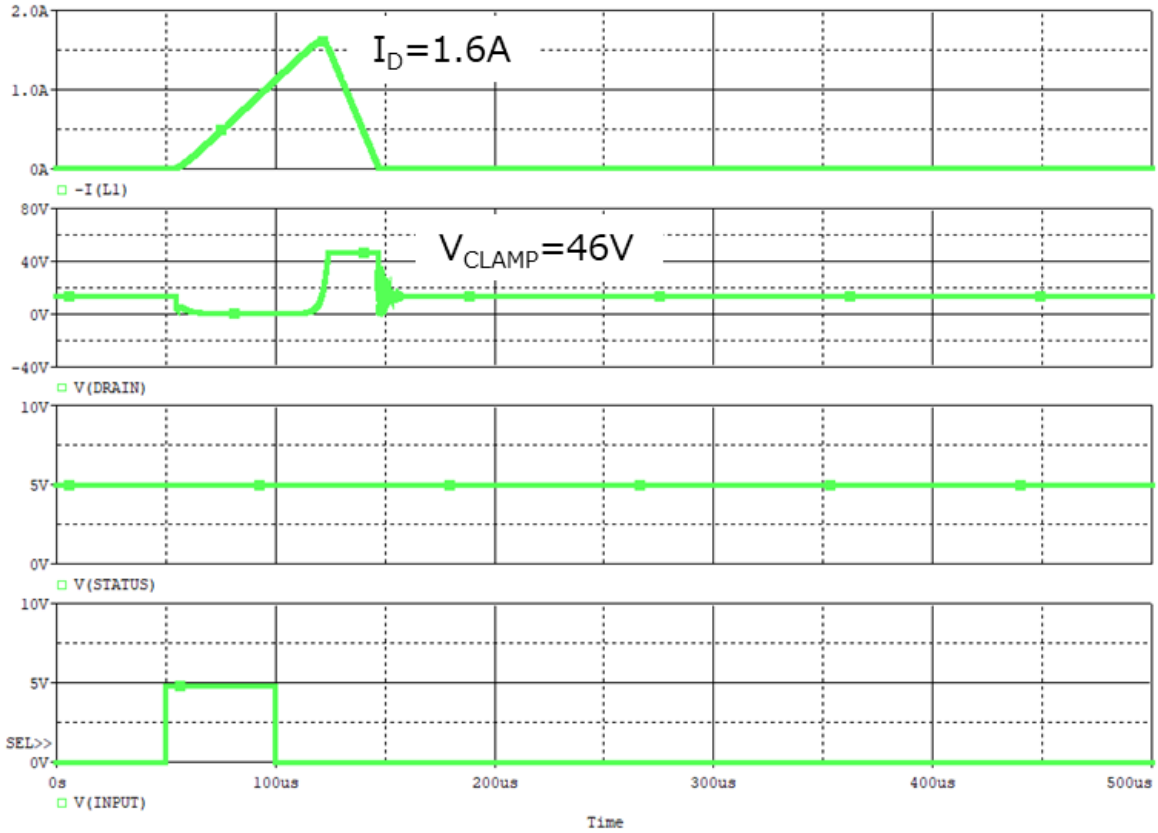


Overvoltage clamp Testbench

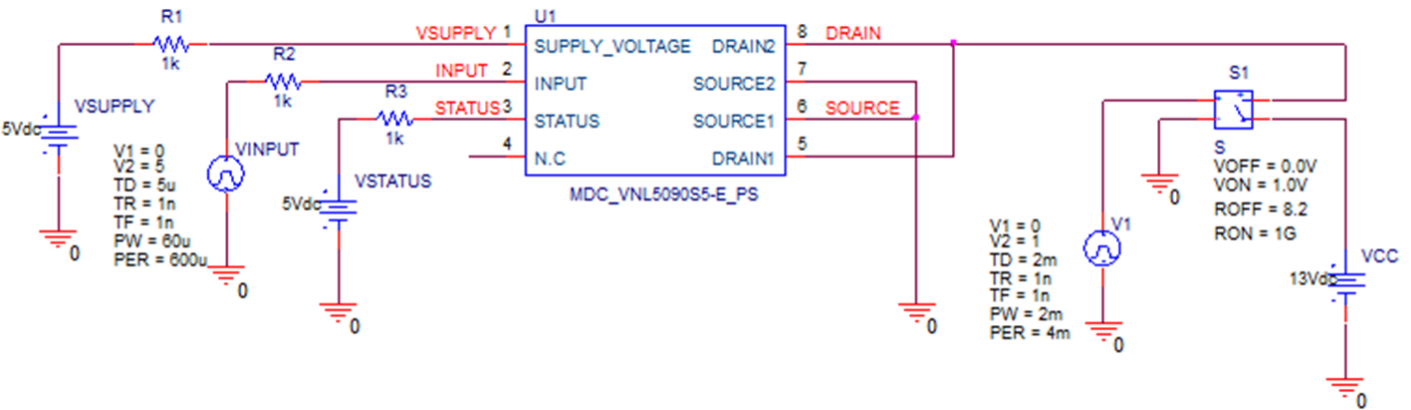


Simulation results are following.  
 Explanatory notes — : simulated

Overvoltage clamp

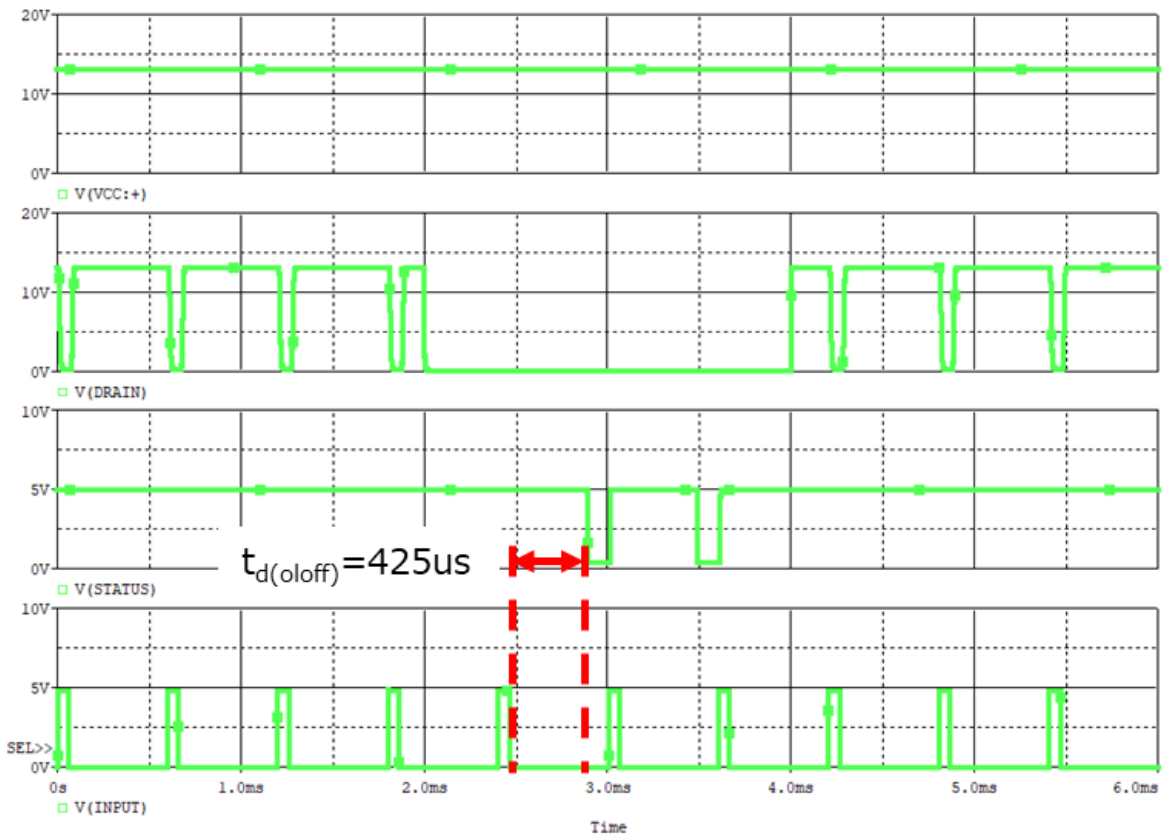


Open load detection Testbench

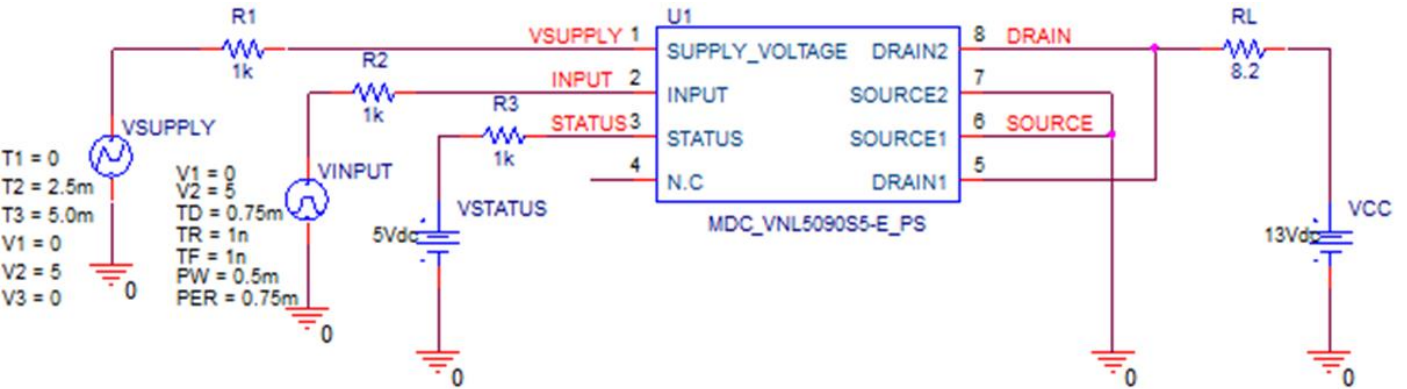


Simulation results are following.  
 Explanatory notes — : simulated

Open load detection

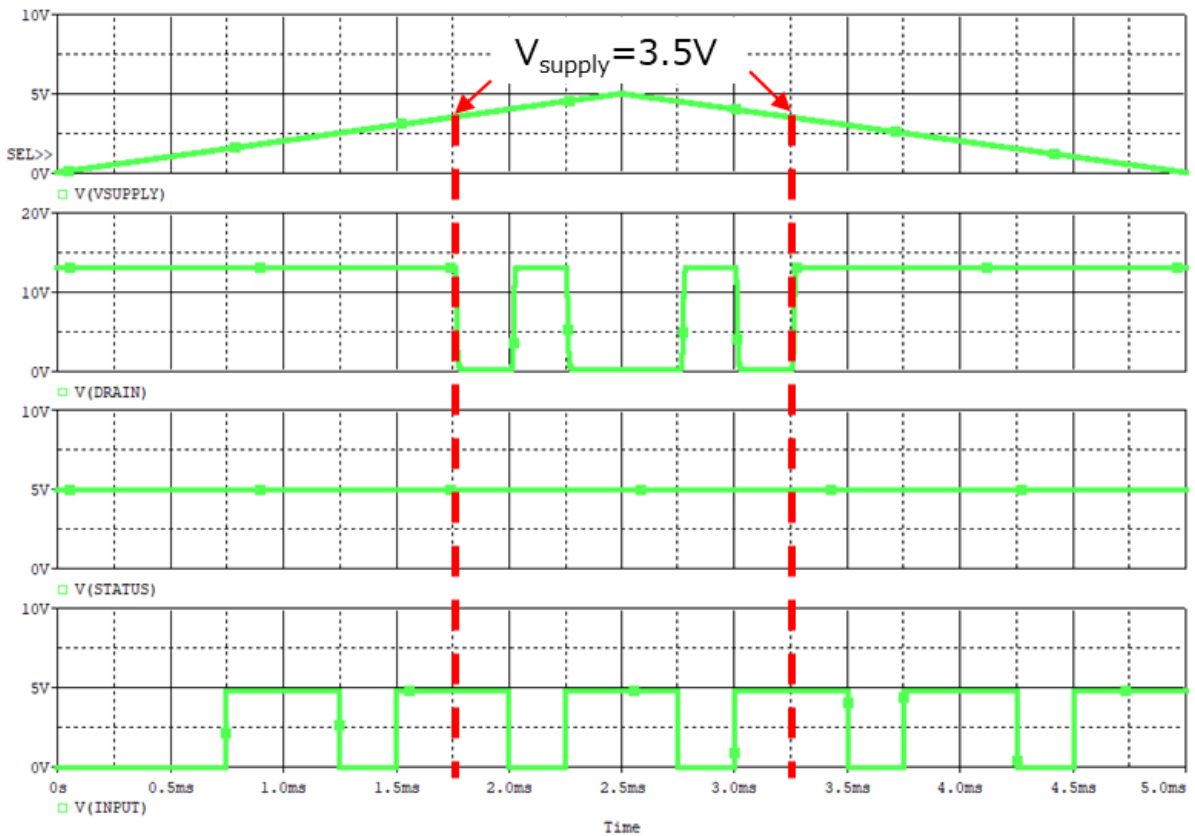


Under voltage Testbench



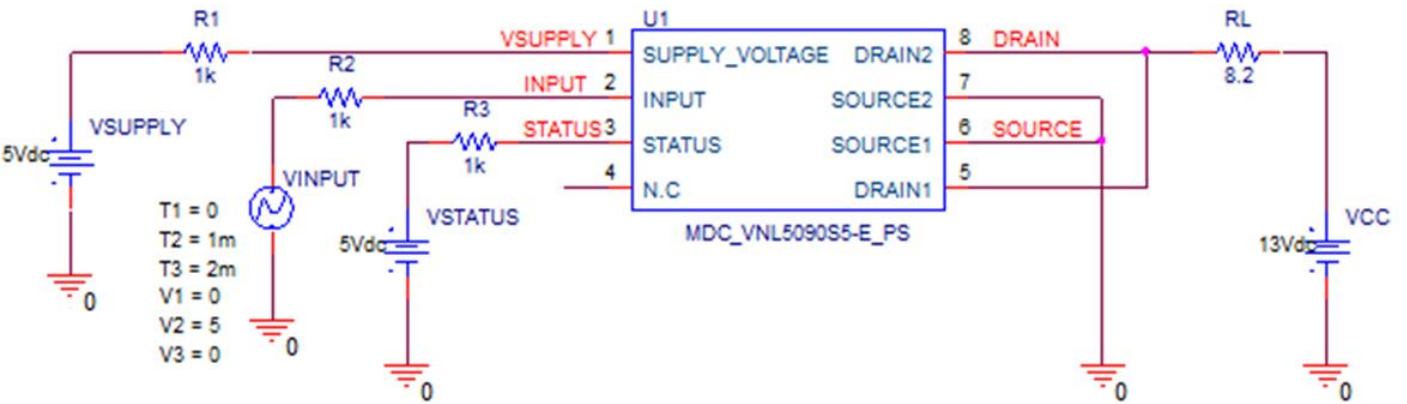
Simulation results are following.  
 Explanatory notes — : simulated

Under voltage



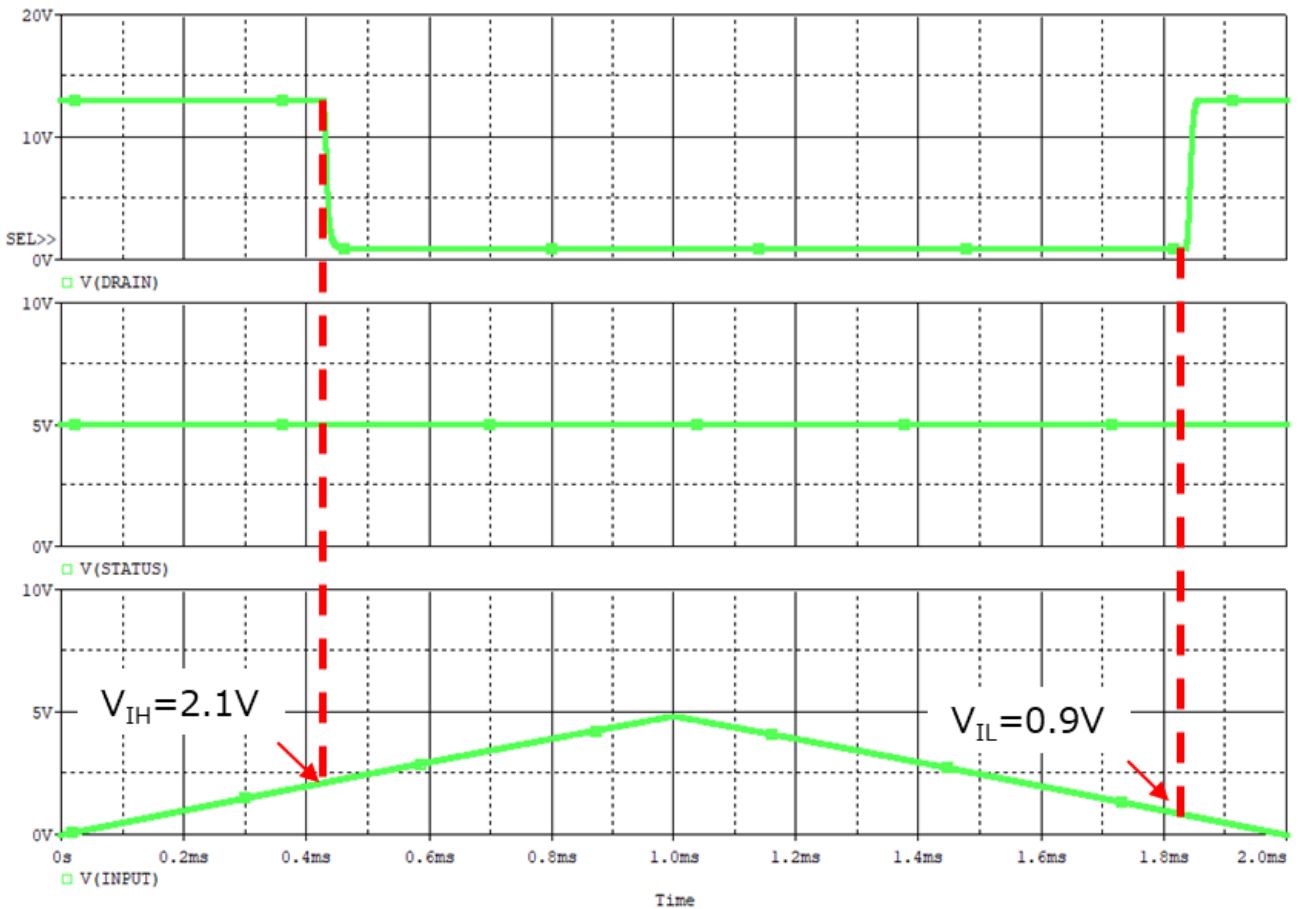


Input Voltage Testbench

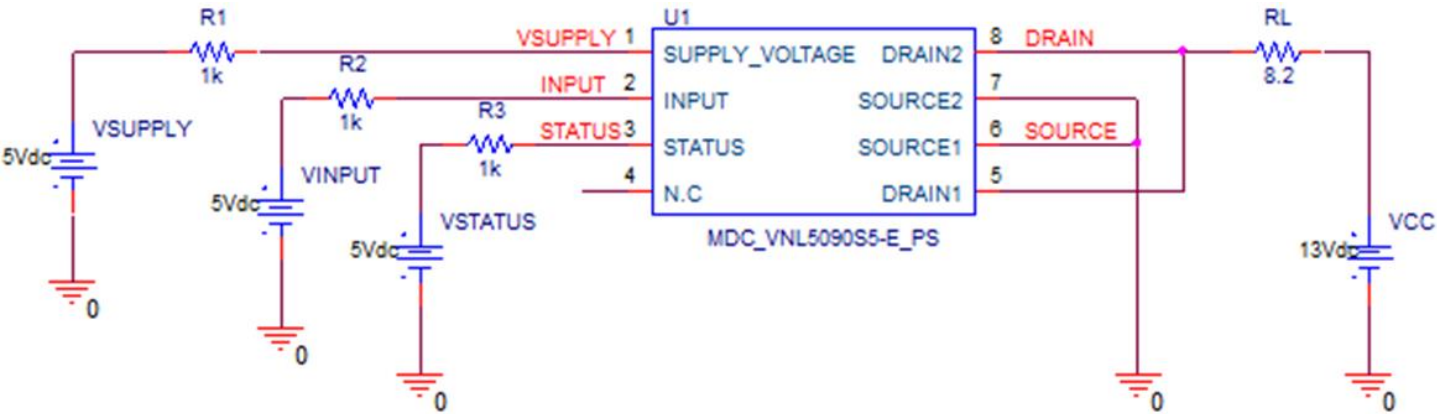


Simulation results are following.  
 Explanatory notes — : simulated

Input Voltage

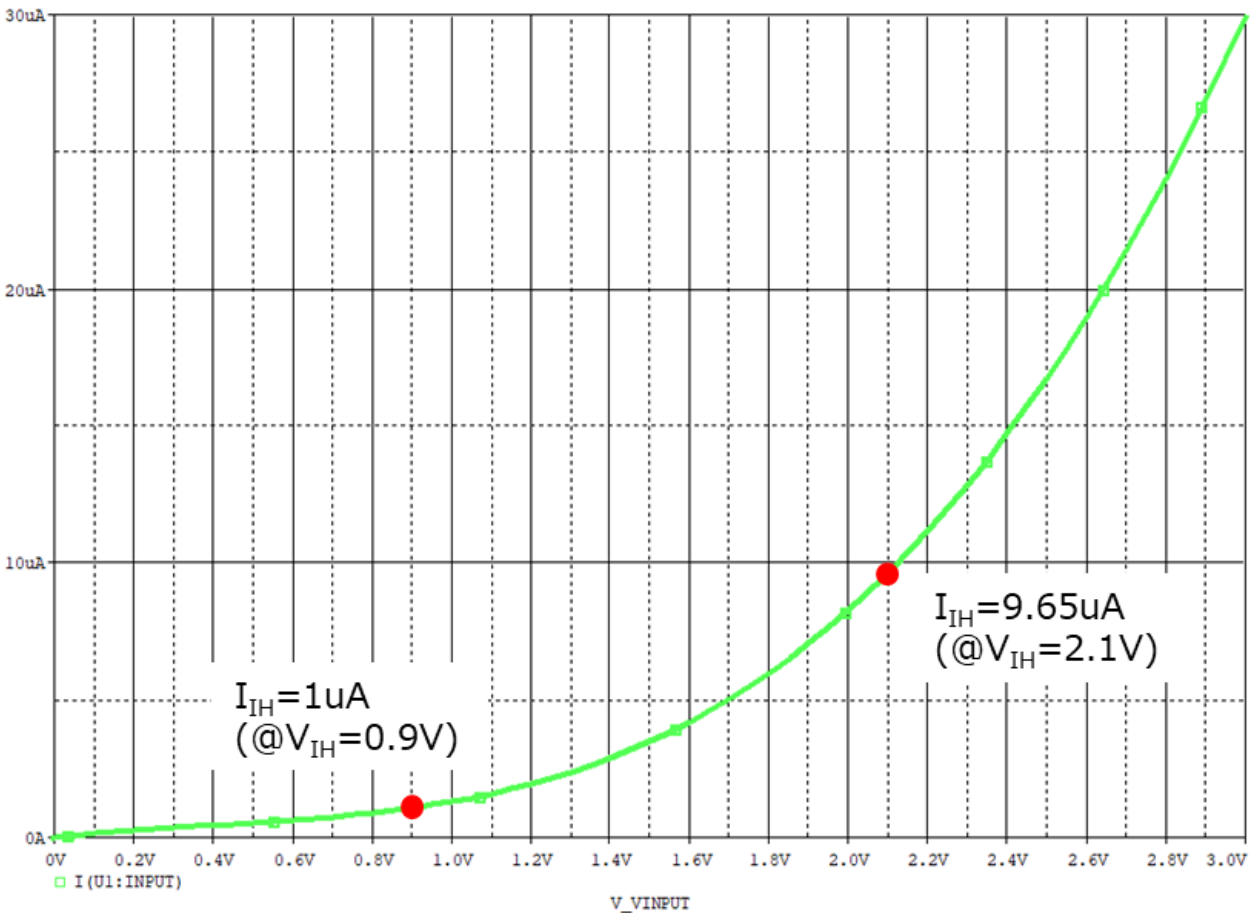


Input Current Testbench

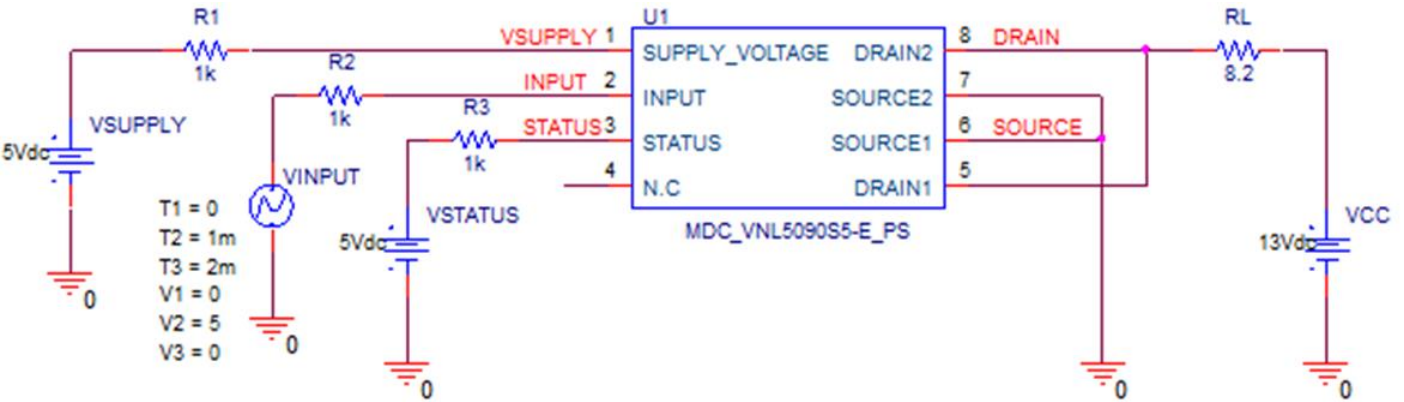


Simulation results are following.  
 Explanatory notes — : simulated

Input Current

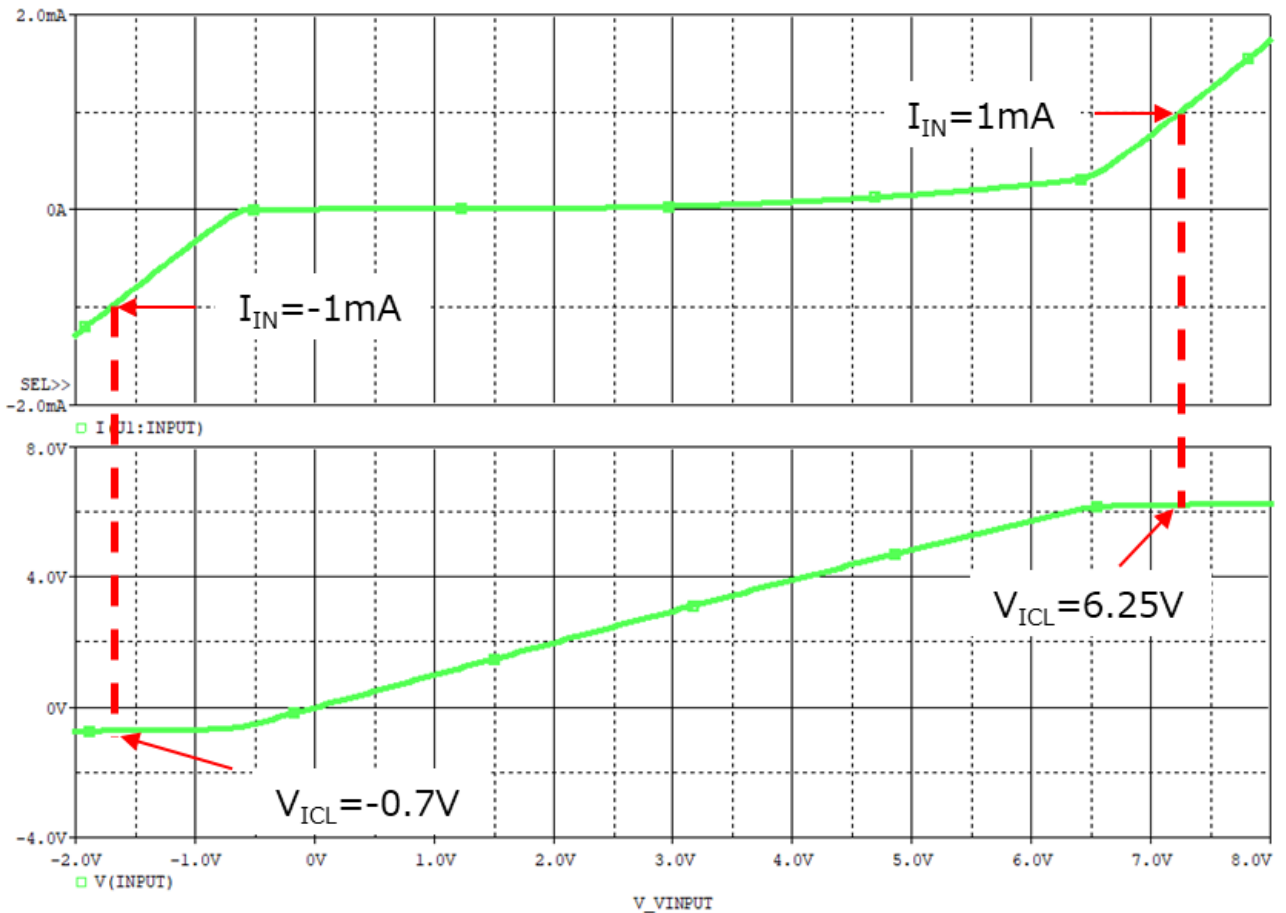


Input Clamp Voltage Testbench

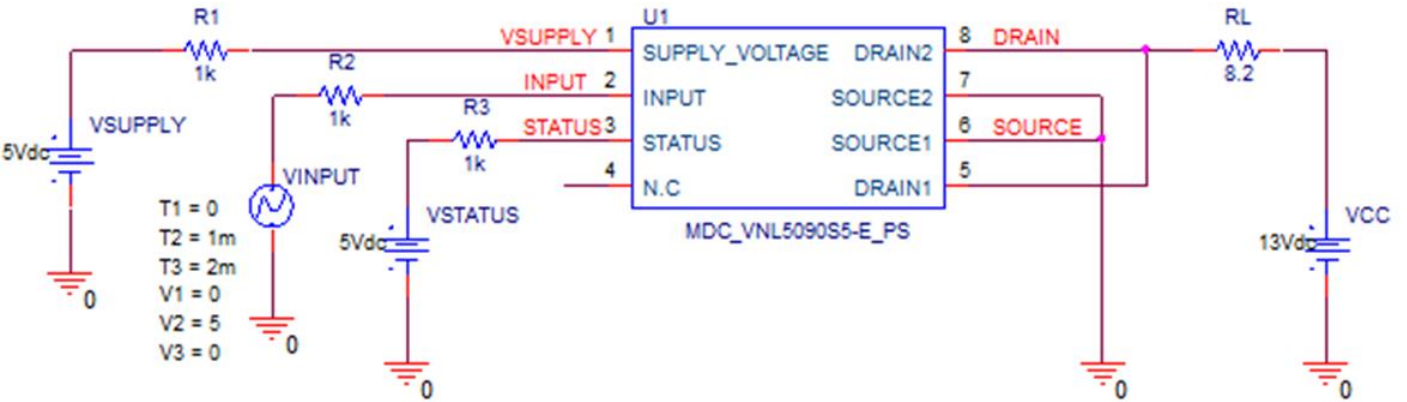


Simulation results are following.  
 Explanatory notes — : simulated

Input Clamp Voltage

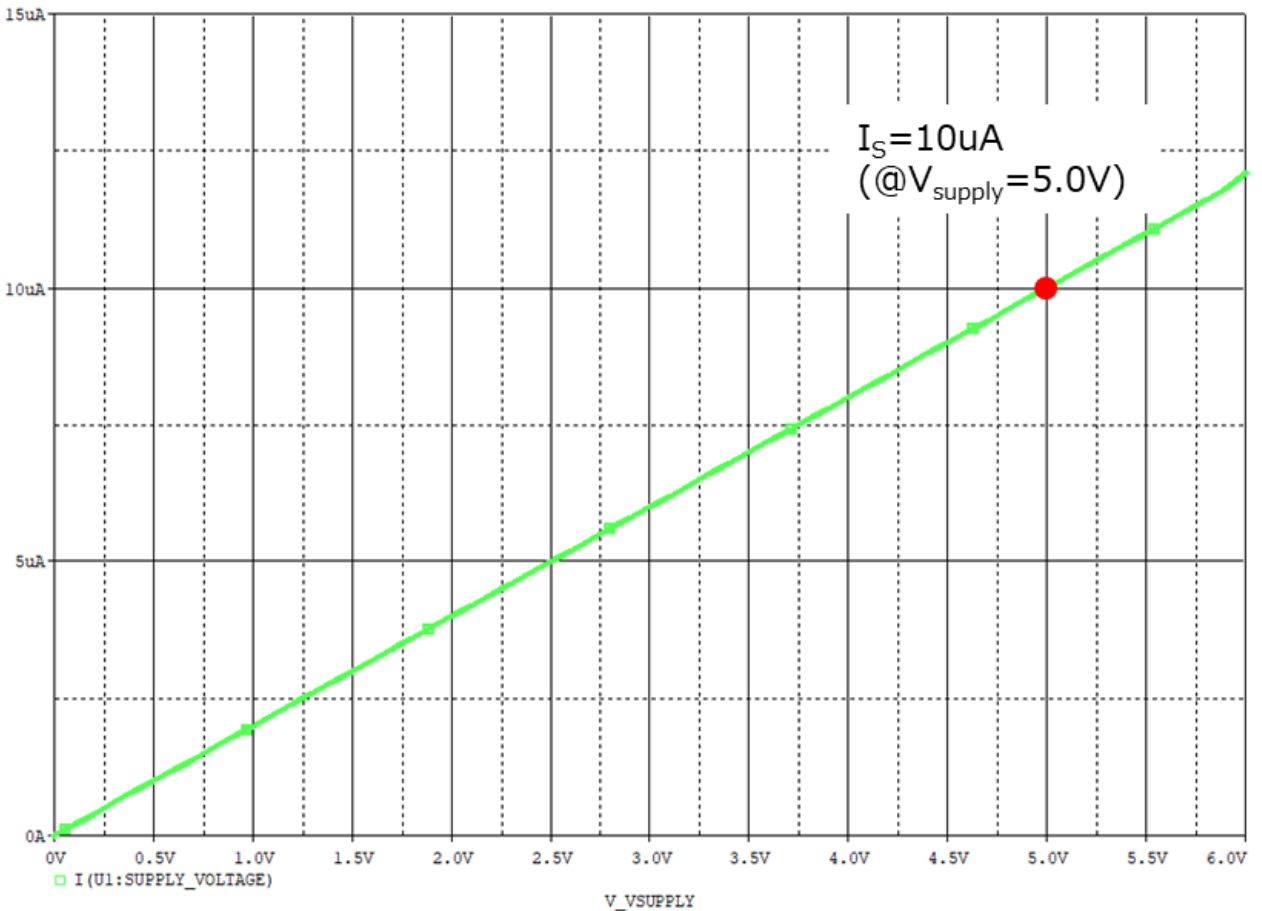


Supply Current off Testbench

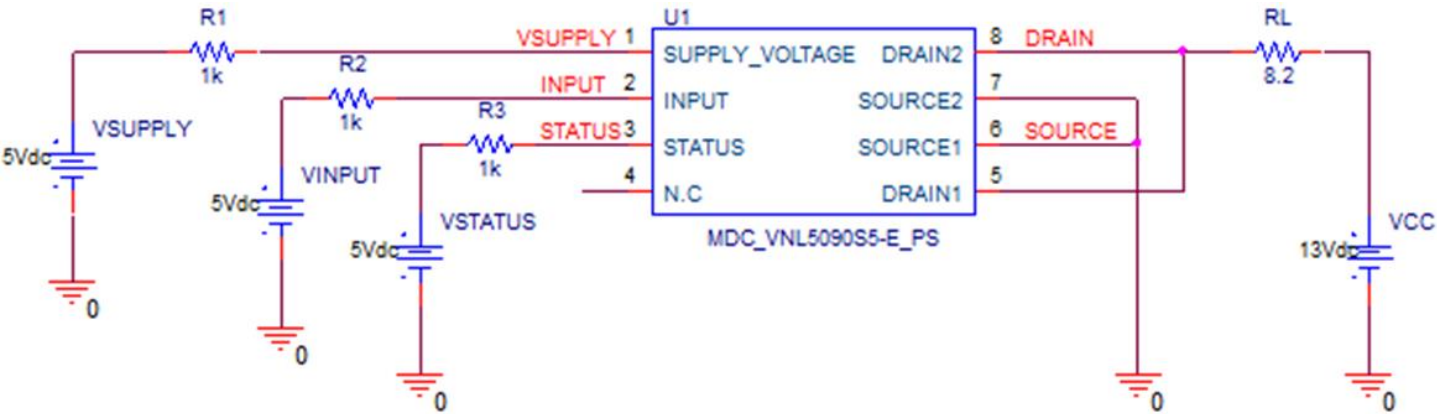


Simulation results are following.  
 Explanatory notes — : simulated

Supply Current off

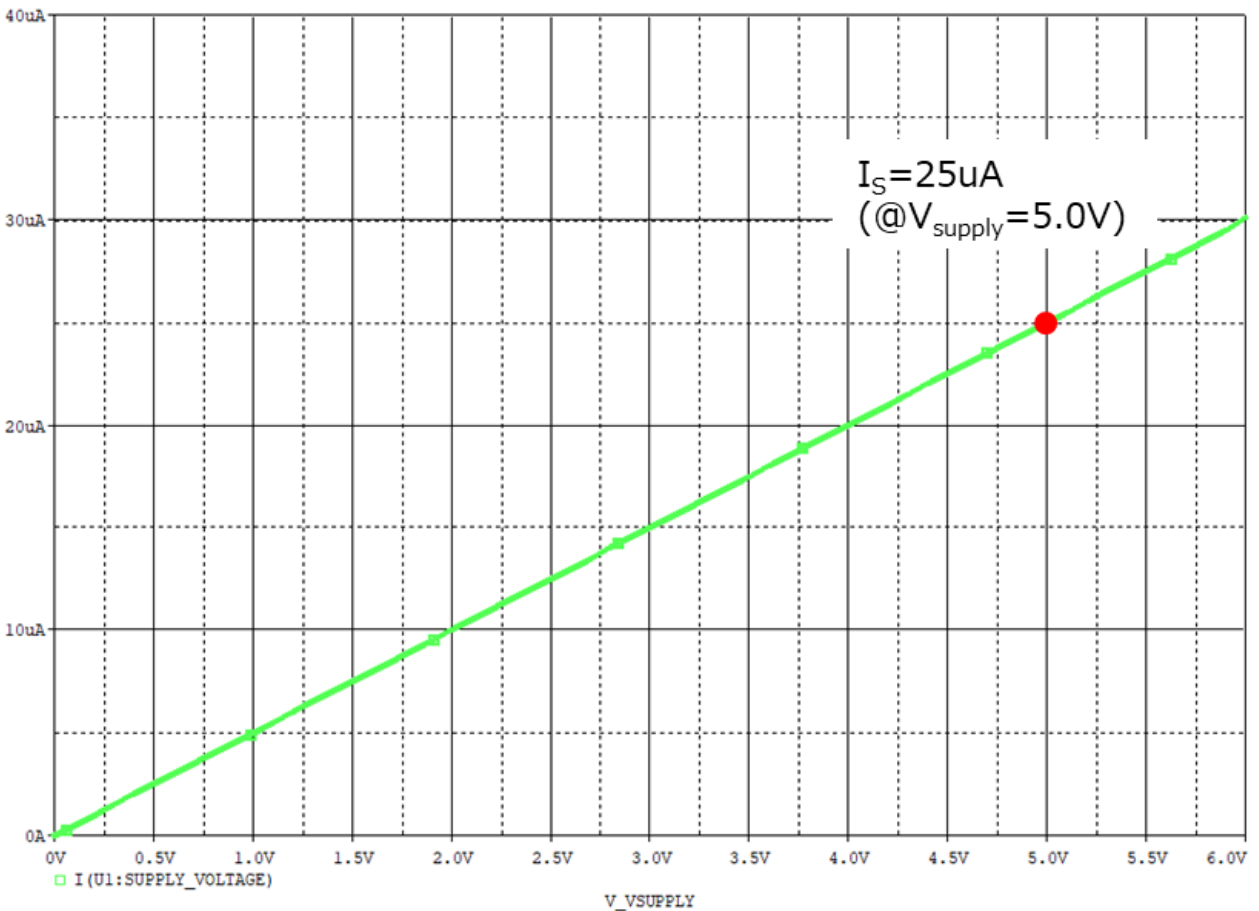


Supply Current on Testbench

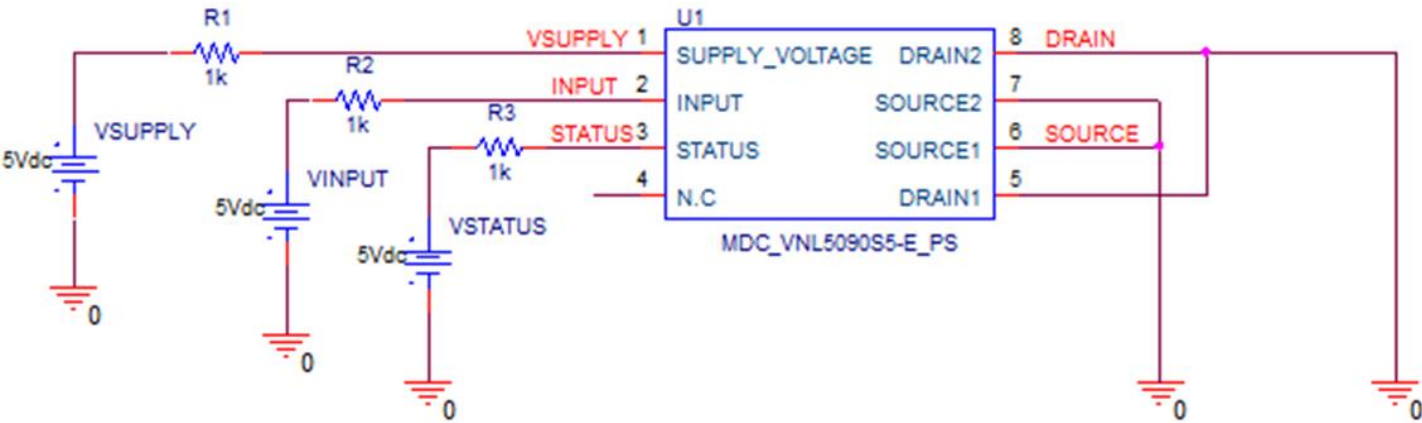


Simulation results are following.  
 Explanatory notes — : simulated

Supply Current on

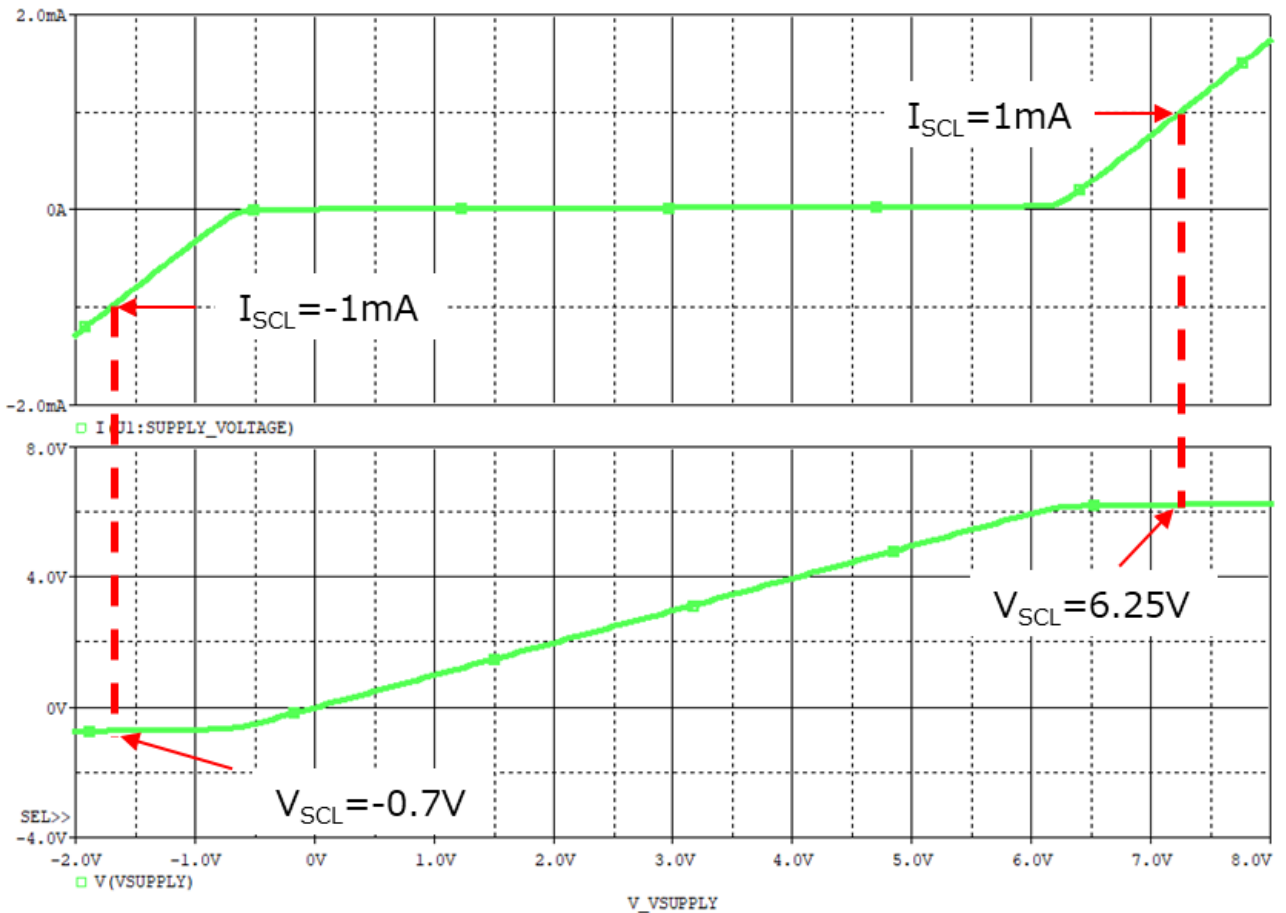


Supply Clamp Voltage Testbench

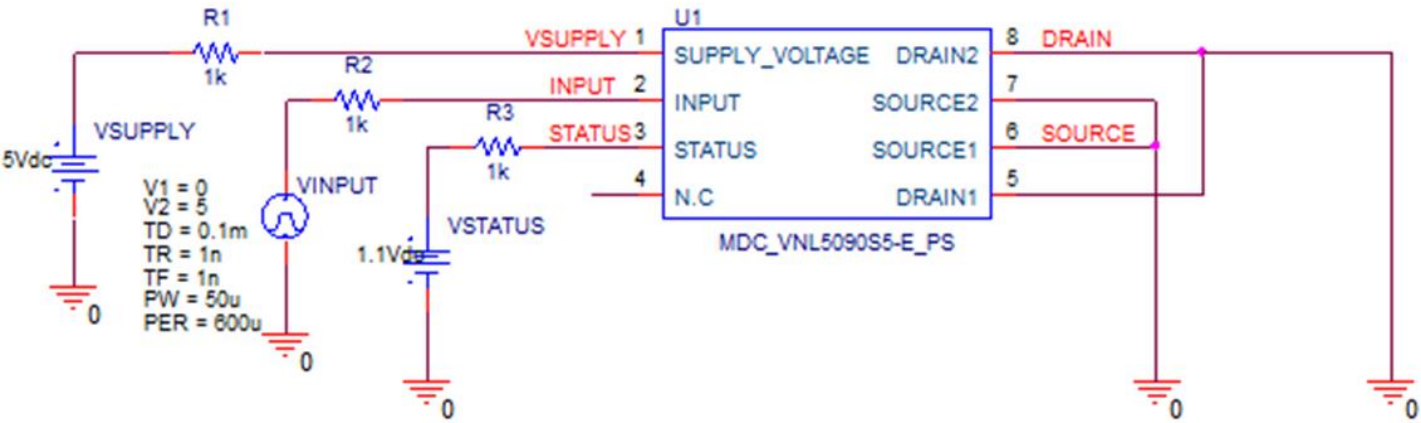


Simulation results are following.  
 Explanatory notes — : simulated

Supply Clamp Voltage

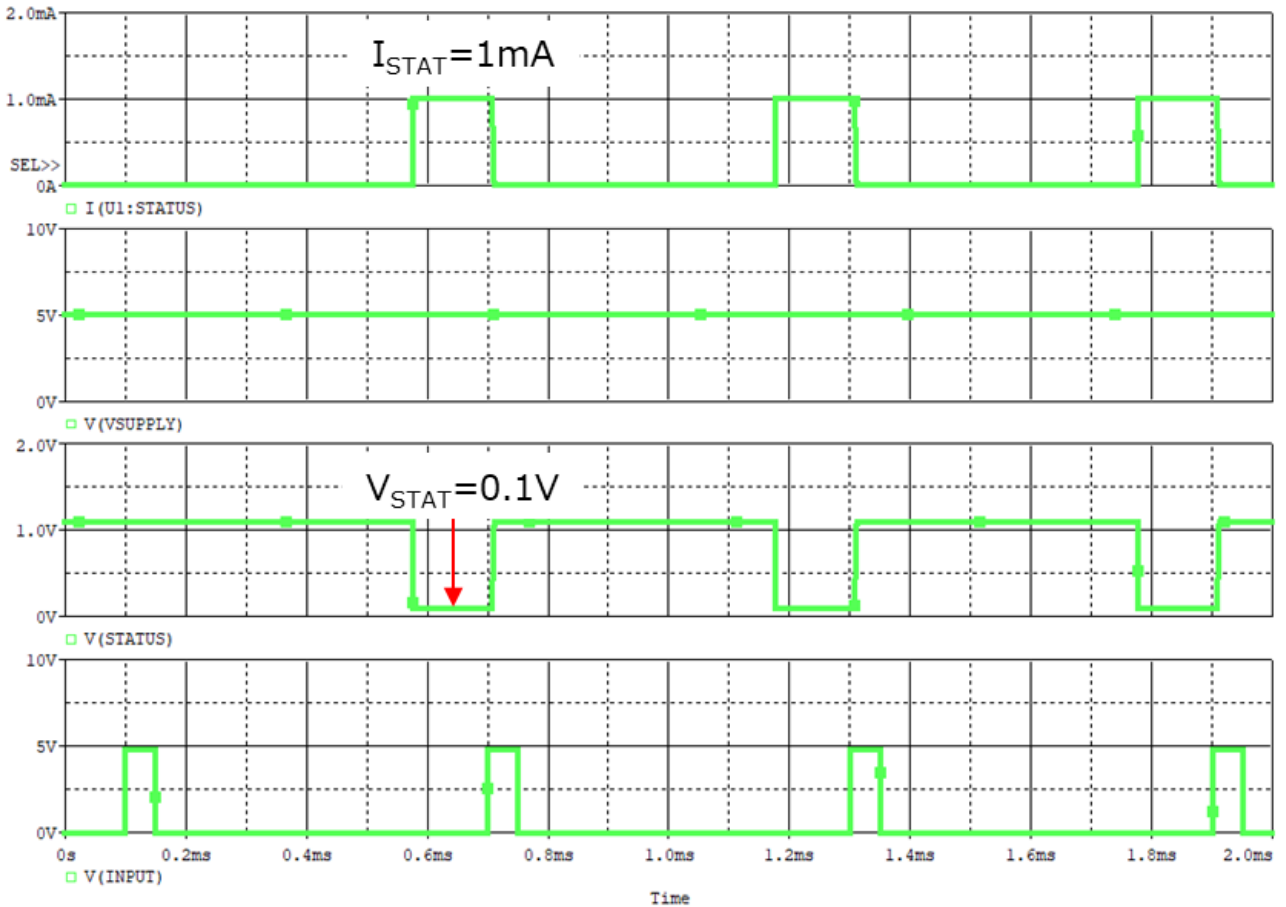


Status Voltage Testbench

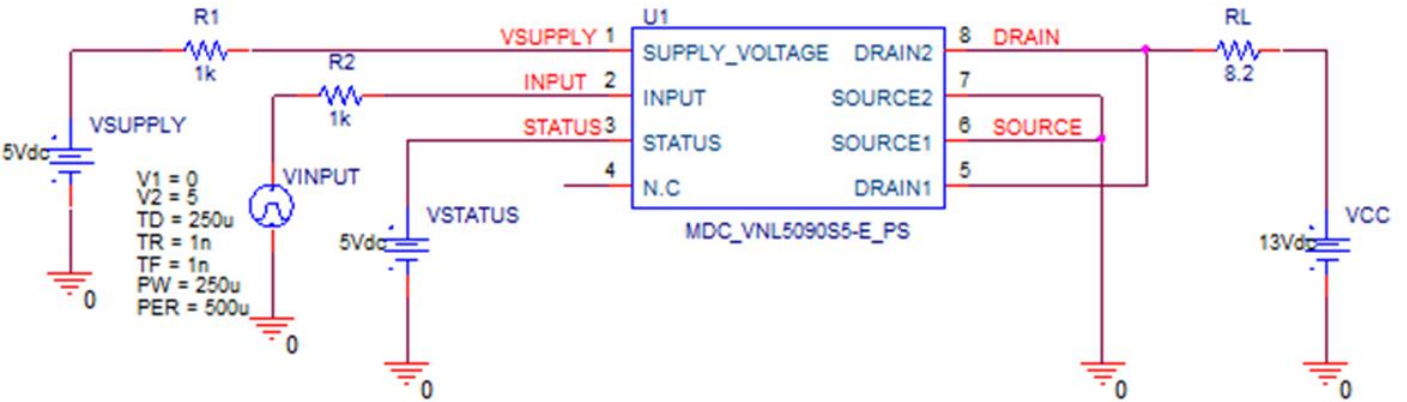


Simulation results are following.  
 Explanatory notes — : simulated

Status Voltage

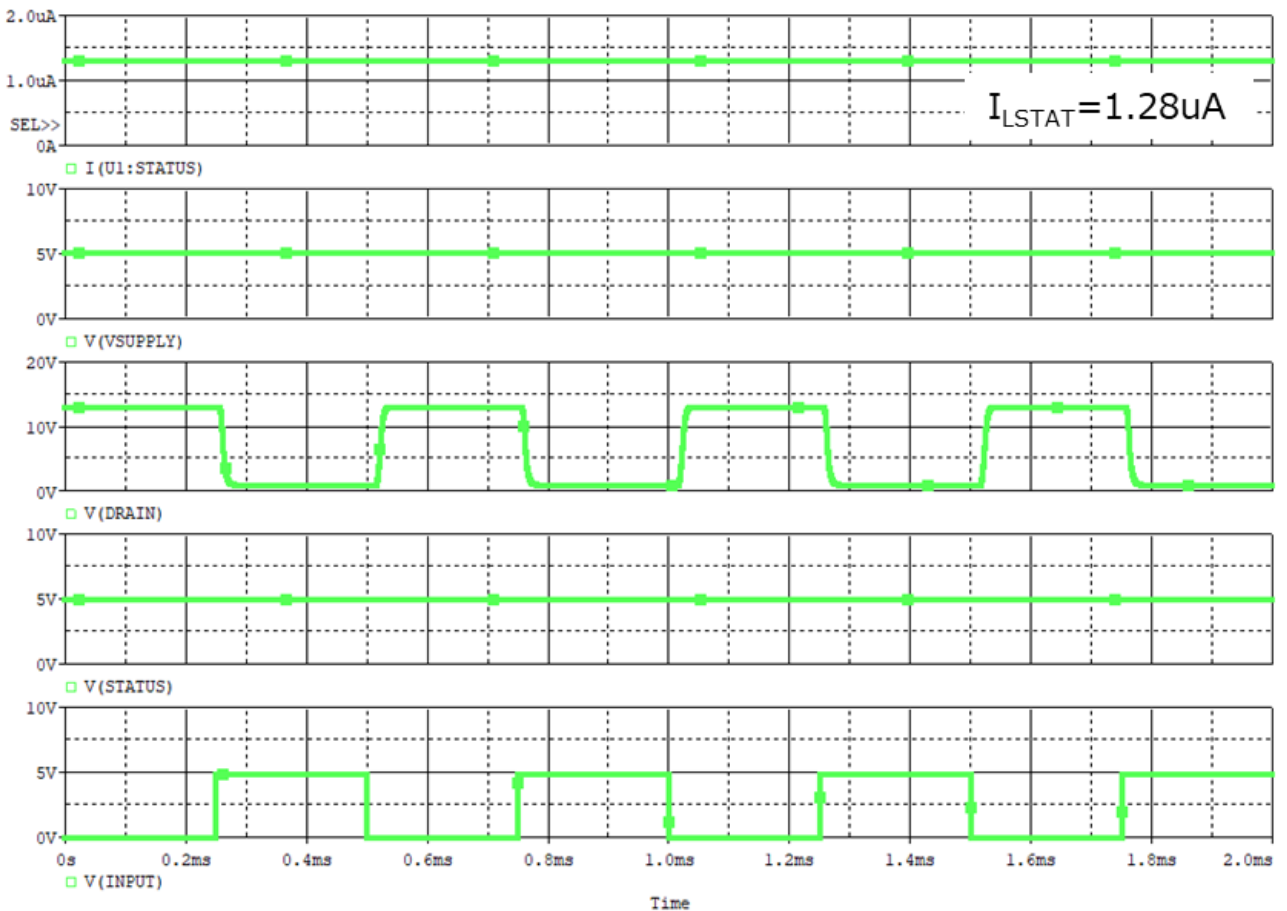


Status Current Testbench



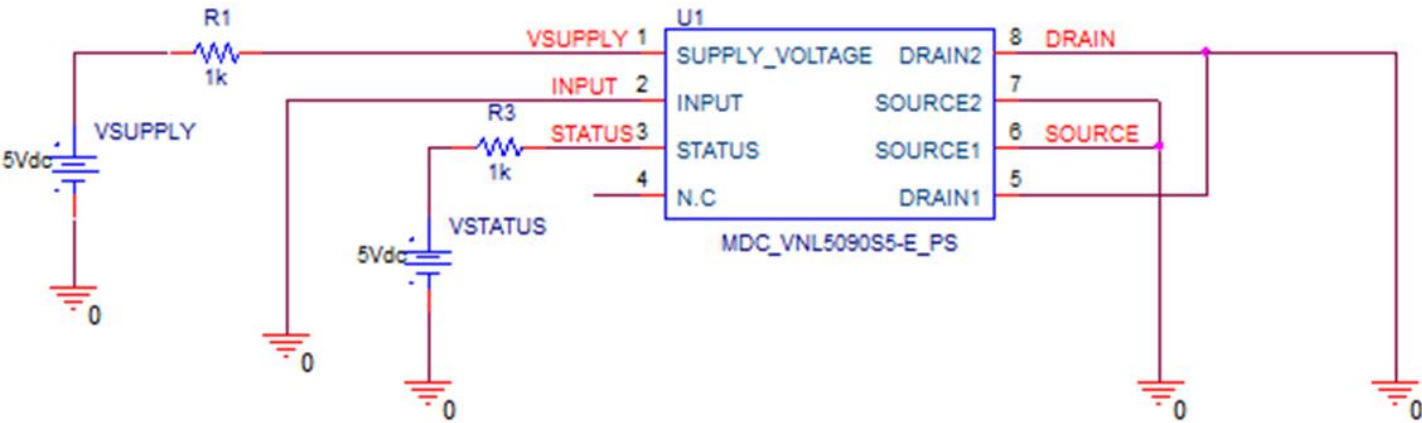
Simulation results are following.  
 Explanatory notes — : simulated

Status Current



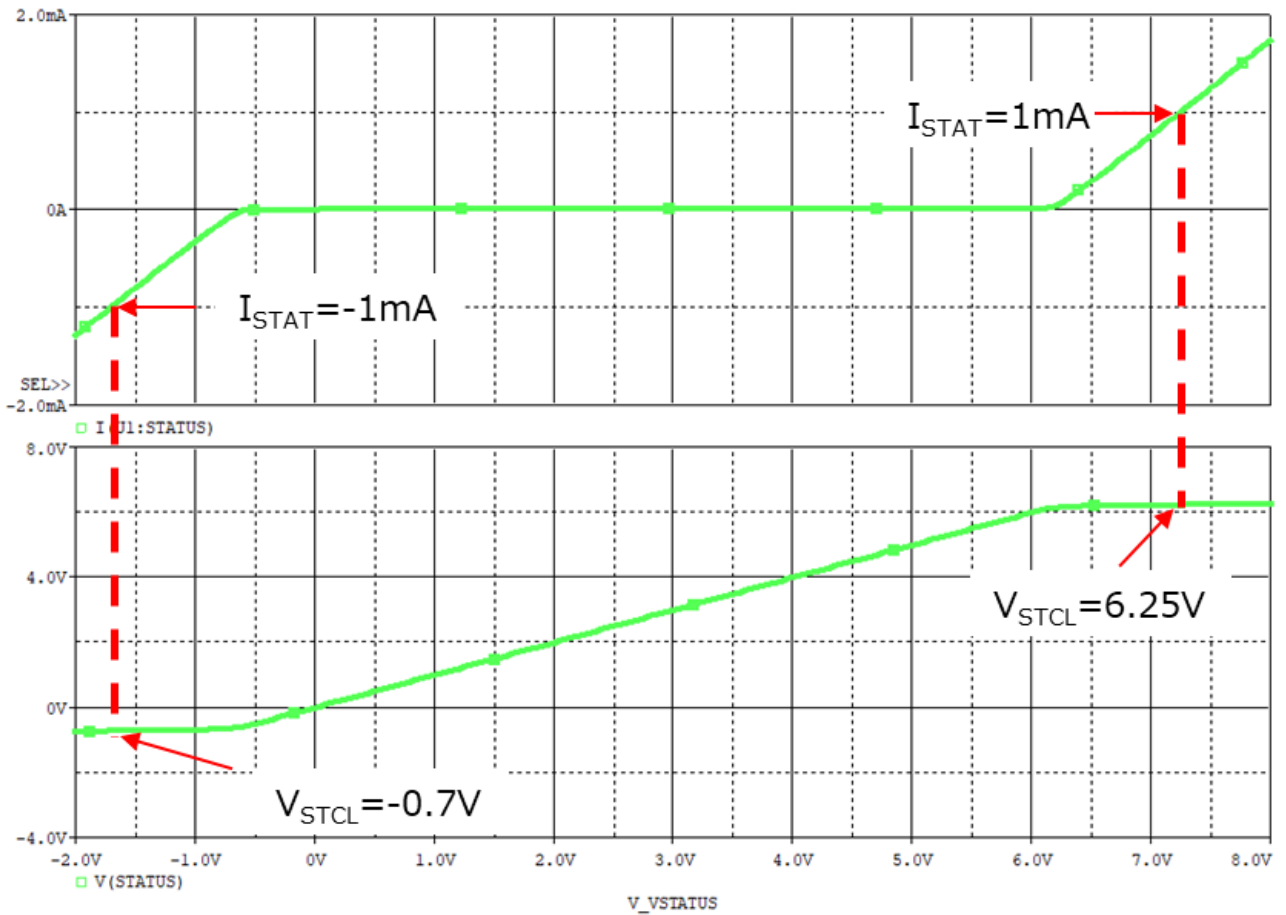


Status Clamp Voltage Testbench



Simulation results are following.  
 Explanatory notes — : simulated

Status Clamp Voltage



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