

# PSpice Model

## Rectifier

### ON Semiconductor

### FES10D

#### Model Information

**Model** A macro model based on general SPICE diode model  
**Call Name** MDC\_FES10D\_PS  
**Pin Assign** 1:Anode1 2:Anode2 3:Cathode  
**File List** Model Library MDC\_FES10D\_PS.lib  
 Model Report MDC\_FES10D\_PS.pdf(this file)  
**Verified Simulator Version** PSpice version 17.4

#### Note

#### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version April, 2020 – Rev. 4
- Product name FES10D
- Company name ON Semiconductor.

[Characteristics listed]

- Characteristics IfVf[Temp], IrVr[Temp], CjVr, trrlflr

#### Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item        | Range |    |      | Unit  |
|-------------|-------|----|------|-------|
|             | Min.  |    | Max. |       |
| Temperature | -55   | to | 150  | deg C |

## Diode

○ : Implemented  
× : Not Implemented  
— : Not applicable

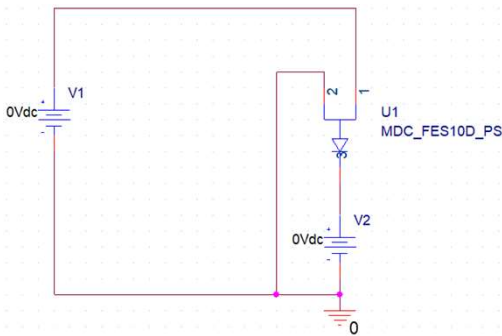
Model Functions Table

RANK=1

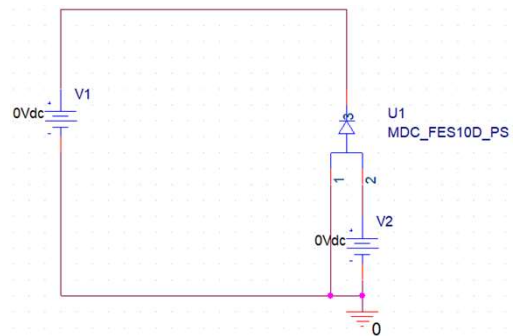
| Functions                             | RANK | Implemented |
|---------------------------------------|------|-------------|
| IF-VF(Temp)                           | 1    | ○           |
| IR-VR(Temp)                           | 1    | ○           |
| Capacitance                           | 1    | ○           |
| Reverse recovery characteristics      | 1    | ○           |
| Rectification characteristics(Bridge) | 1    | —           |
| Surge voltage-Transient               | 2    | —           |

**IfVf[Temp], IrVr[Temp] Testbench  
Referred to Data Sheet**

**IfVf[Temp]**

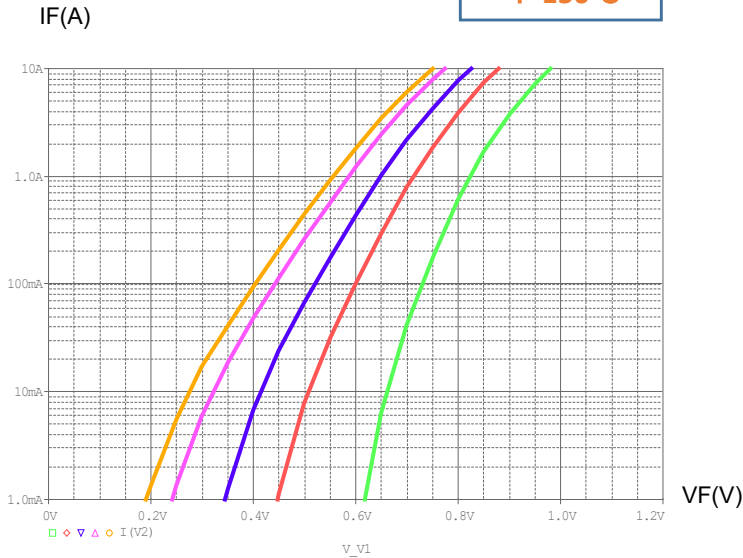
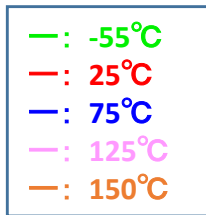


**IrVr[Temp]**

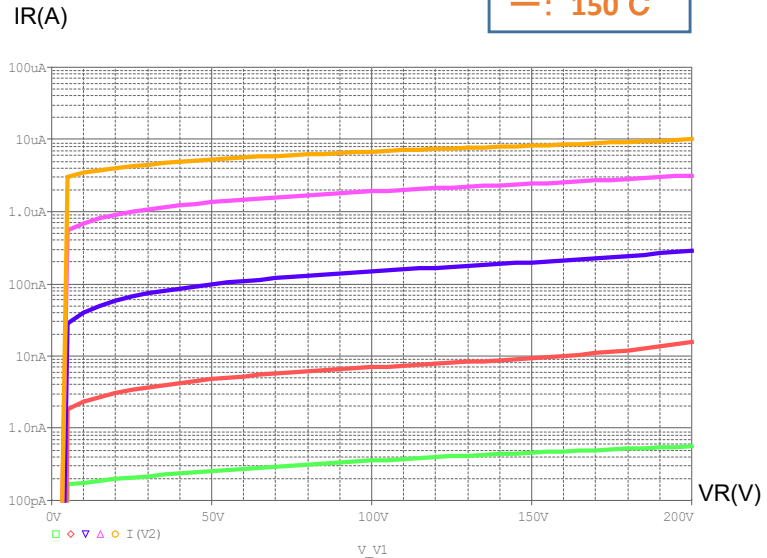
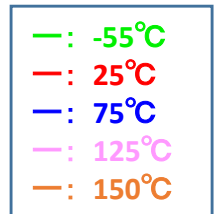


Simulation results are following.  
Explanatory notes — : simulated

**IfVf[Temp]**



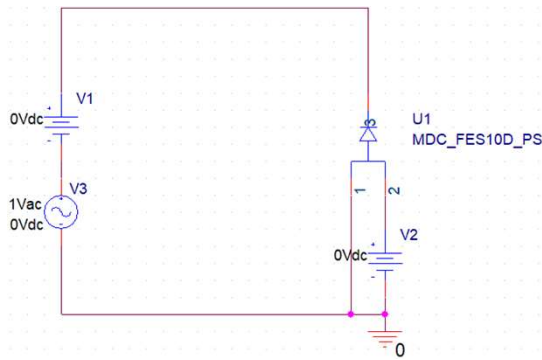
**IrVr[Temp]**



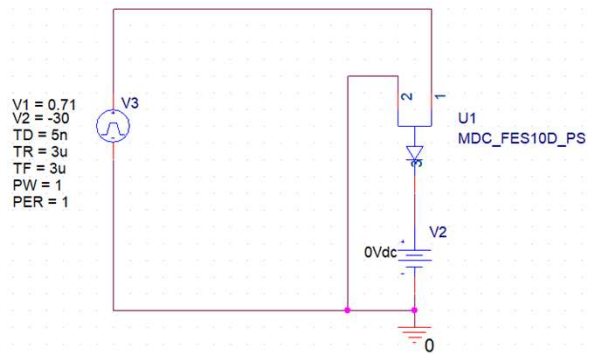
**CjVr, trrlflr Testbench**

**Referred to Data Sheet**

**CjVr**

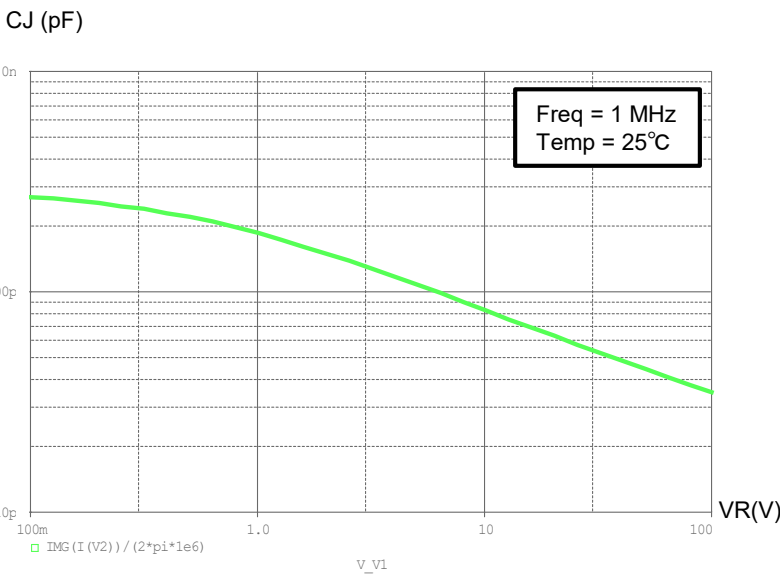


**trrlflr**

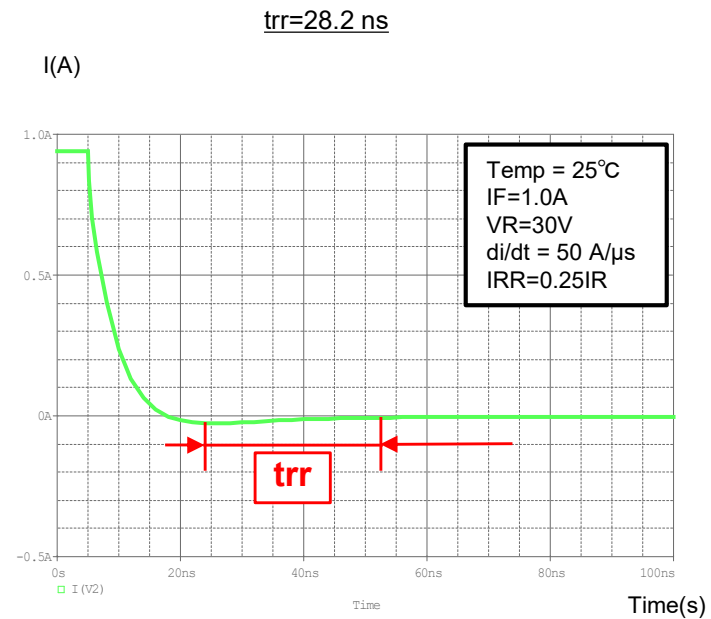


Simulation results are following.  
Explanatory notes — : simulated

**CjVr**



**trrlflr**



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