

LTspice Model LDO Torex Semiconductor XC6222D181PR-G

Model Information

Model A macro model

Call Name MDC_XC6222D181PR-G_LT Pin Assign 1:CE 2:VSS 3:NC 4:VIN 5:VOUT

File List Model Library MDC_XC6222D181PR-G_LT03.lib

Model Report MDC_XC6222D181PR-G_LT.pdf(this file)

Verified Simulator Version LTspice XVII

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version N/A

Product nameCompany nameXC6222D181PR-GTorex Semiconductor

[Characteristics listed]

Characteristics
 VIN-VOUT, Limit Current, Dropout Voltage
 Line Regulation, Load Regulation, CE

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C



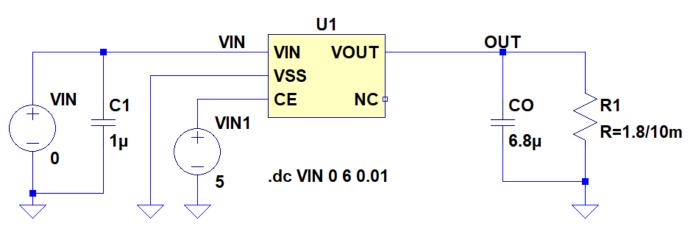
Model Functions Table

Functions	Implemented
VIN-VOUT	0
Limit Current	0
Dropout Voltage	0
Line Regulation	0
Load Regulation	0
CE	0



VIN-VOUT Testbench

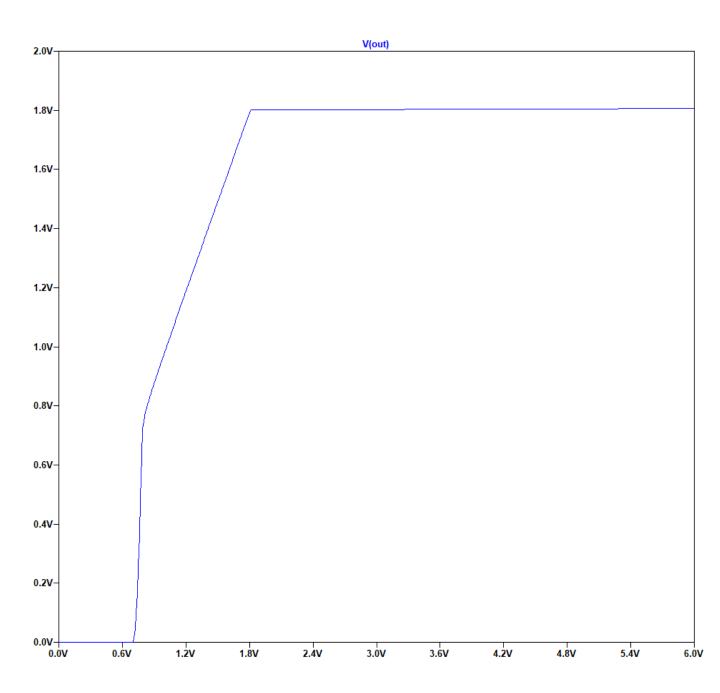
Referred to Data Sheet



.lib MDC_XC6222D181PR-G_LT.lib



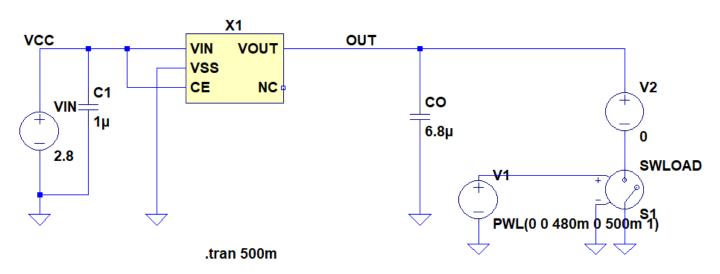
VIN-VOUT





Limit Current Testbench

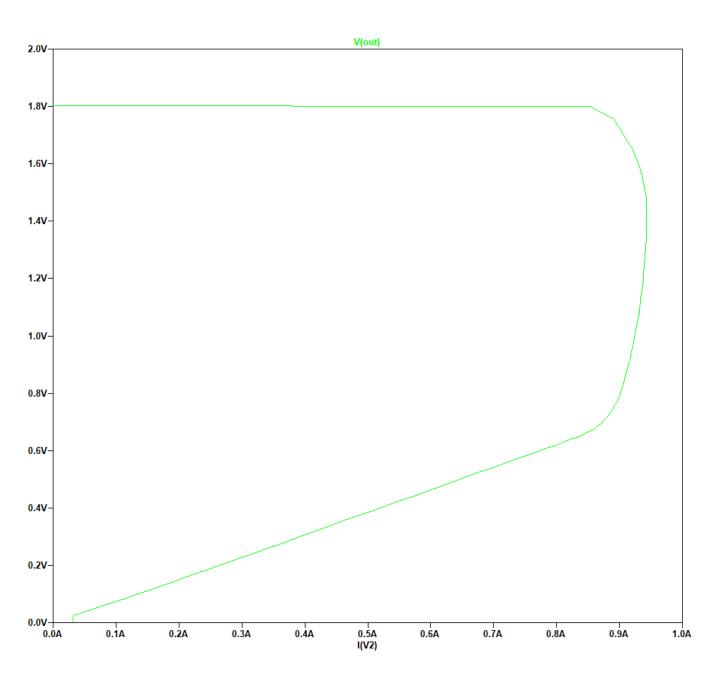
Referred to Data Sheet



.MODEL SWLOAD SW RON=1m ROFF=1Meg VON=1 VOFF=0
.lib MDC_XC6222D181PR-G_LT.lib



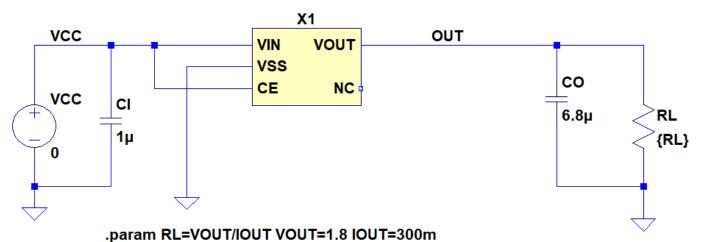
Limit Current





Dropout Voltage Testbench

Referred to Data Sheet



.dc VCC 0 2.8 0.001

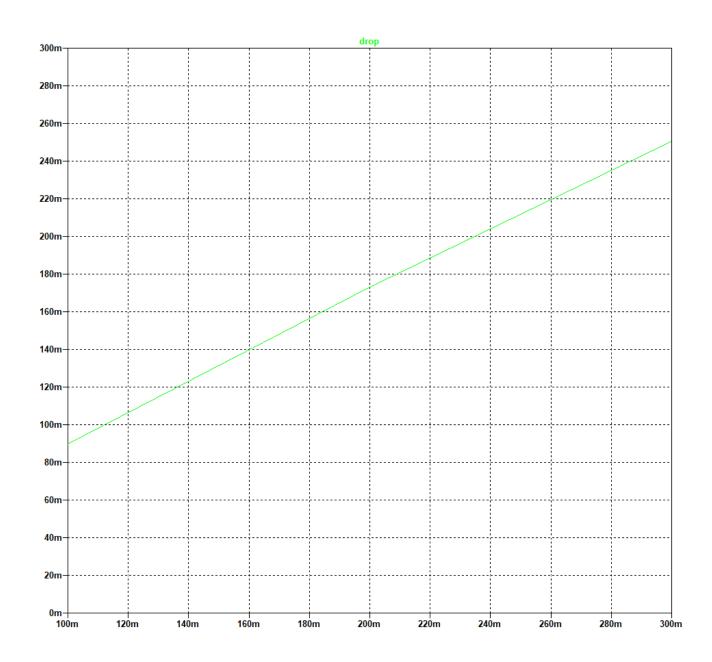
.step param IOUT 100m 300m 100m

.meas DC drop FIND V(VCC)-V(OUT) WHEN V(OUT)=1.7 RISE=1

.lib MDC_XC6222D181PR-G_LT.lib



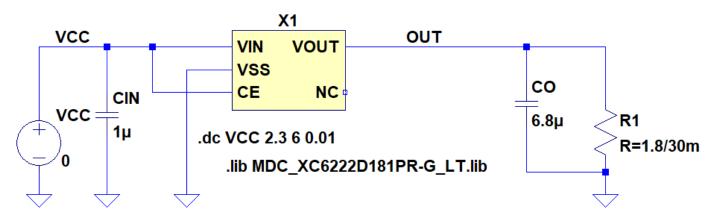
Dropout Voltage





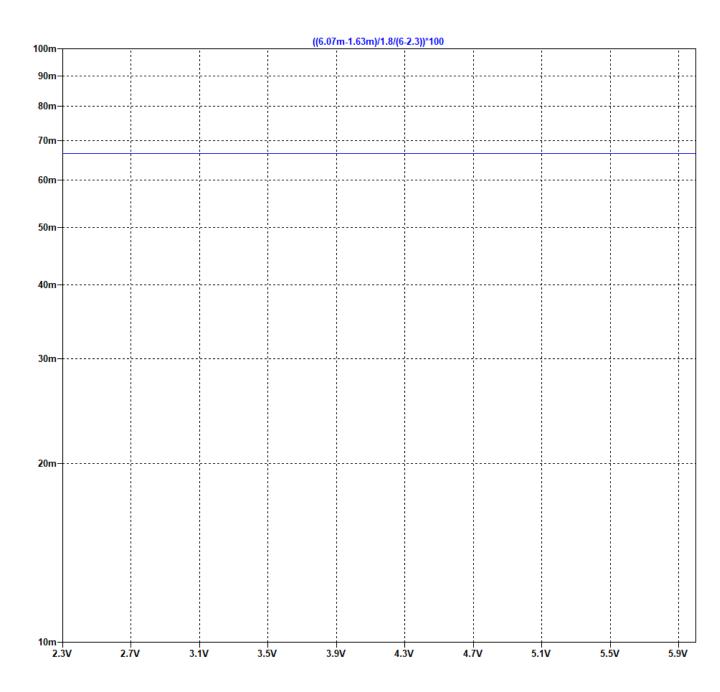
Line Regulation Testbench

Referred to Data Sheet





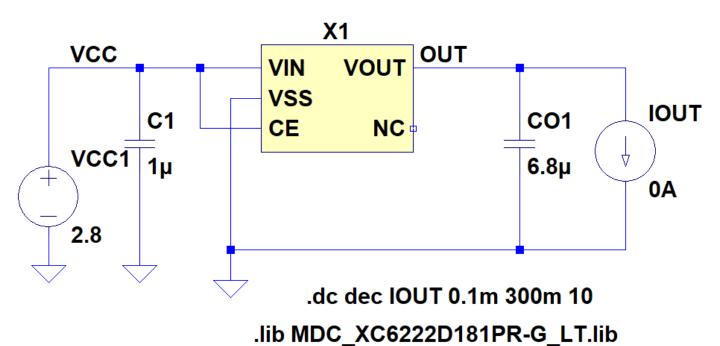
Line Regulation





Load Regularion Testbench

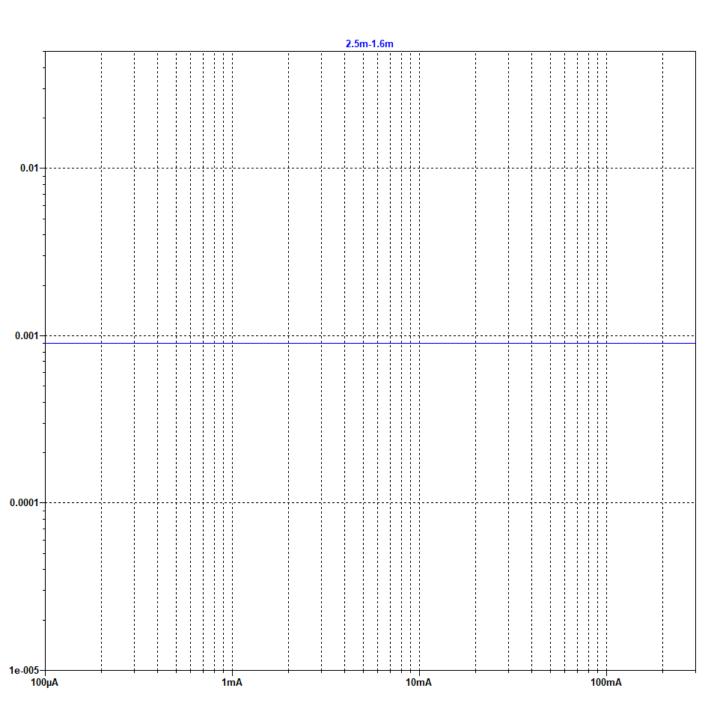
Referred to Data Sheet



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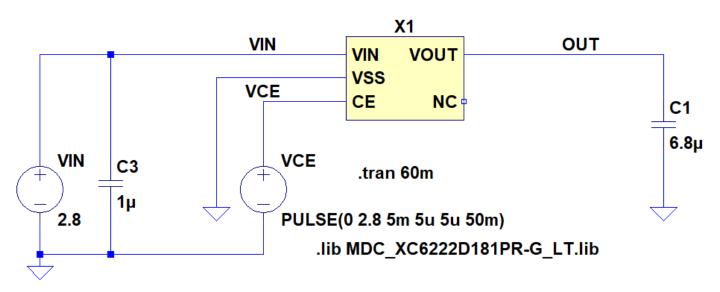
Road Regulation





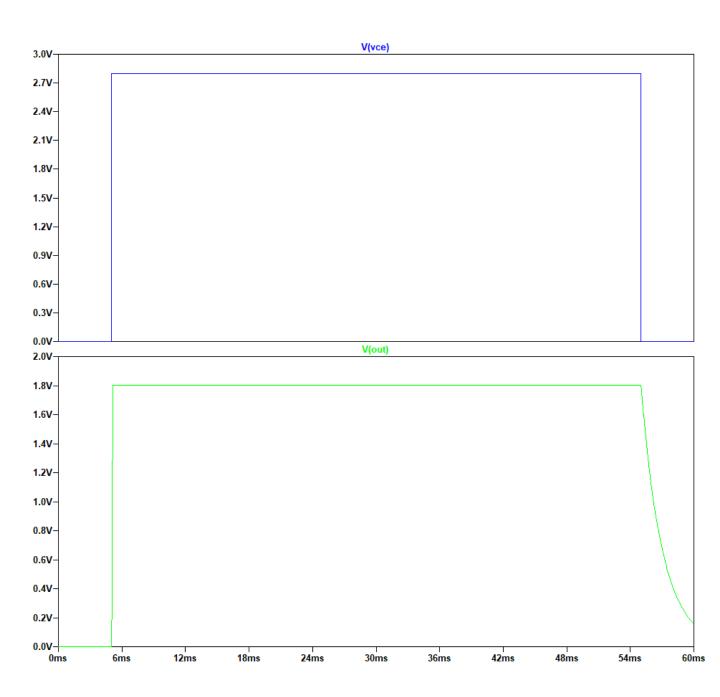
CE Testbench

Referred to Data Sheet





CE





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