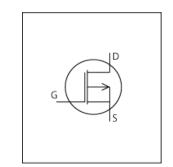


# LTspice Model PMOS ON FQB9P25TM



# **Model Information**

Model A macro model based on BSIM3 model

Call Name MDC\_FQB9P25TM\_LT Pin Assign 1:G 2:NC 3:S 4:D

File List Model Library MDC\_FQB9P25TM\_LT02.lib

Model Report MDC\_FQB9P25TM\_LT.pdf (this file)

**Verified Simulator Version** 

Note

LTspice version XVII

#### References

The information which was used for modeling is as follow:

[Data Sheet]

Date/VersionProduct nameCompany nameRev.C0FQB9P25TMON Semiconductor.

● Characteristics IdVds[Vgs],IdVgs[Temp],Rds(on)Id[Vgs],IsVsd[Temp],Crss,C

oss, Ciss, VgsQg[Vdd], Rds(on)Temp[Id], tdon, tdoff, tf, tr

### **Simulation Range**

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-250	V
Gate-source voltage (DC)	0	to	-30	V
Temperature	-55	to	150	deg C

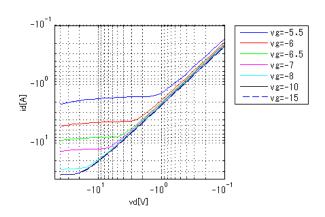


Simulation results are following.

Explanatory notes — : simulated

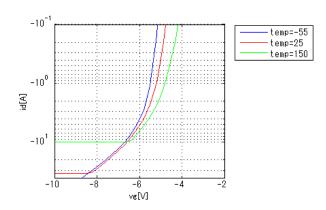
## IdVds[Vgs]

Temp. = 25deg C

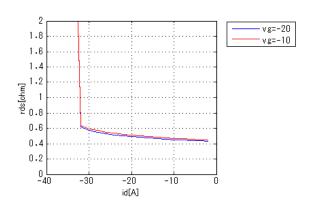


# IdVgs[Temp]

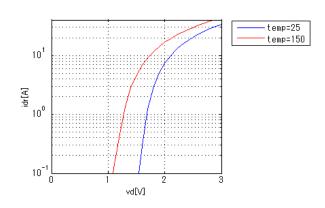
Vds = -50V



# Rds(on)Id[Vgs]

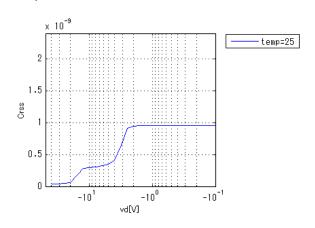


## IsVsd[Temp]



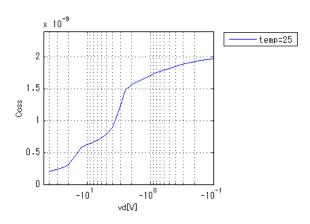
## **Crss**

Freq. = 1MHz



# Coss

Freq. = 1MHz



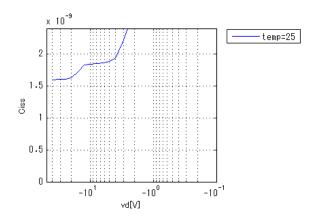


Simulation results are following.

Explanatory notes — : simulated

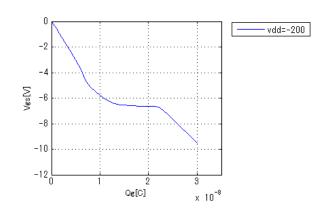
## Ciss

Freq. = 1MHz



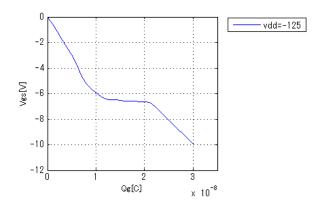
# VgsQg[Vdd]

Id = -9.4A



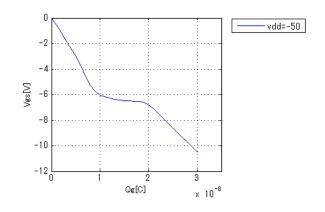
# VgsQg[Vdd]

Id = -9.4A



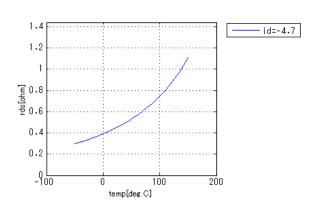
# VgsQg[Vdd]

Id = -9.4A



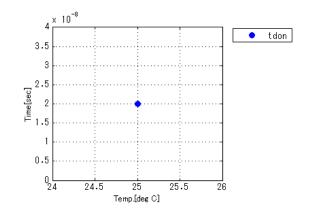
## Rds(on)Temp[Id]

Vgs = -10V



### tdon

Vdd = -125V, Id = -9.4A, +Vg = 0V, -Vg = -10V, Rg = 250hm

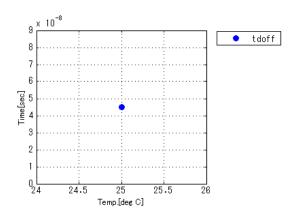




# Simulation results are following. Explanatory notes — : simulated

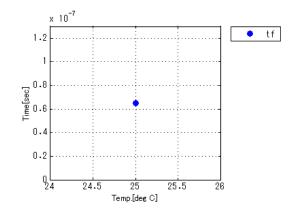
#### tdoff

Vdd = -125V, Id = -9.4A, +Vg = 0V, -Vg = -10V, Rg = 25ohm



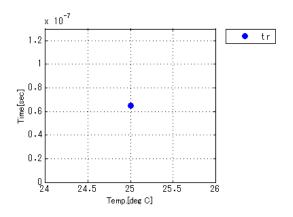
#### tf

Vdd = -125V, Id = -9.4A, +Vg = 0V, -Vg = -10V, Rg = 25ohm



## tr

Vdd = -125V, Id = -9.4A, +Vg = 0V, -Vg = -10V, Rg = 25ohm





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Rev. 1.0