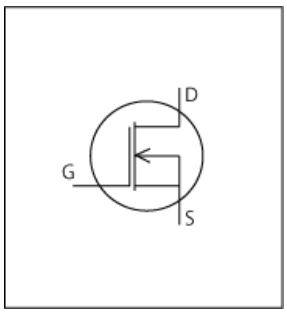
LTspice Model
NMOS
ON Semiconductor
NVMTS0D7N06CL



Model Information

Model	A macro model based on BSIM3 model	
Call Name	MDC_NVMTS0D7N06CL_LT	
Pin Assign	1:G 2:S 3:S 4:S 5:D 6:D 7:D 8:D	
File List	Model Library	MDC_NVMTS0D7N06CL_LT01.lib
	Model Report	MDC_NVMTS0D7N06CL_LT.pdf (this file)
Verified Simulator Version		LTspice version XVII
Note		

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version Rev.2
- ●Product name NVMTS0D7N06CL
- ●Company name ON Semiconductor.
- ●Characteristics IdVds[Vgs],IdVgs[Temp],Rds(on)Id[Vgs],Rds(on)Temp[Id], Rds(on)Vgs[Temp],Crss,Coss,Ciss,VgsQg[Vdd],IsVsd[Temp], tdon,tdoff,tf,tr

Simulation Range

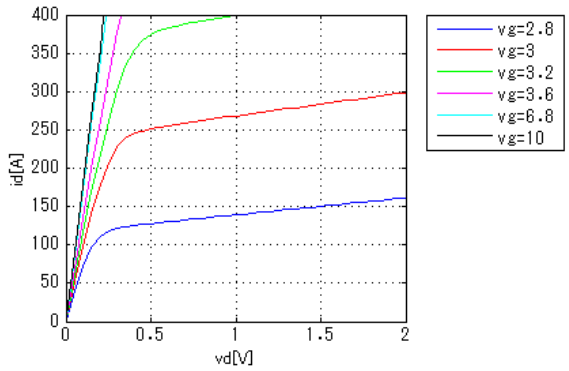
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	0	to	20	V
Temperature	-55	to	175	deg C

Simulation results are following.
Explanatory notes — : simulated

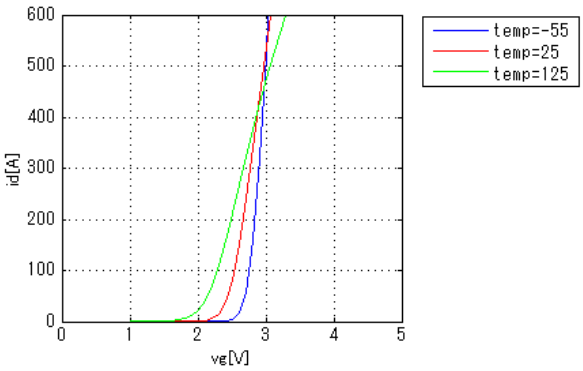
IdVds[Vgs]

Temp. = 25deg C

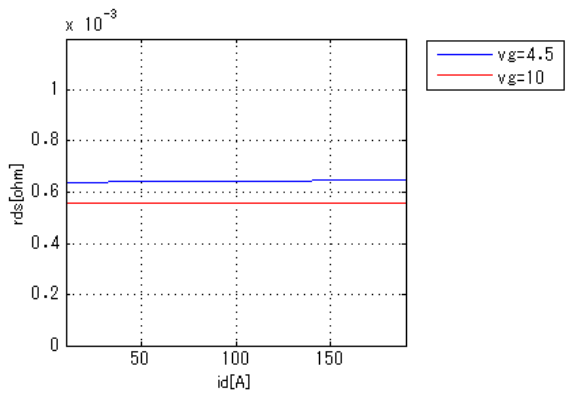


IdVgs[Temp]

Vds = 10V

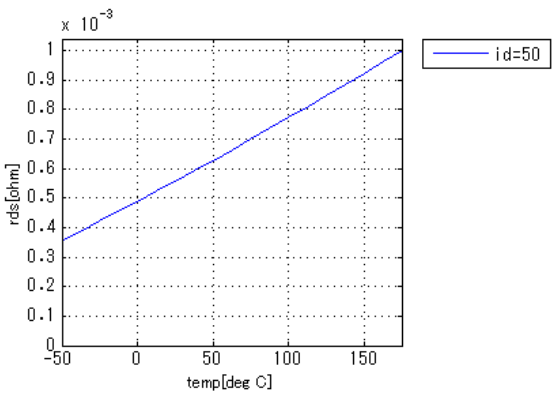


Rds(on)Id[Vgs]



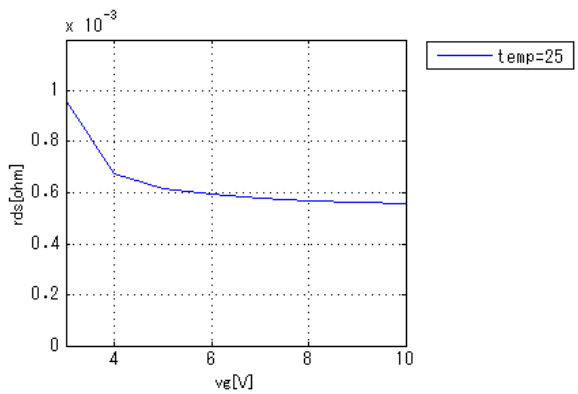
Rds(on)Temp[Id]

Vgs = 10V



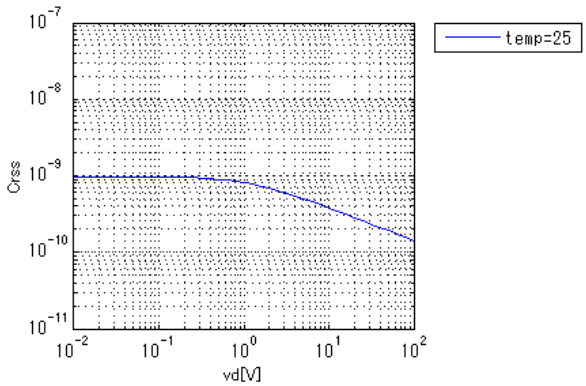
Rds(on)Vgs[Temp]

Id = 50A



Crss

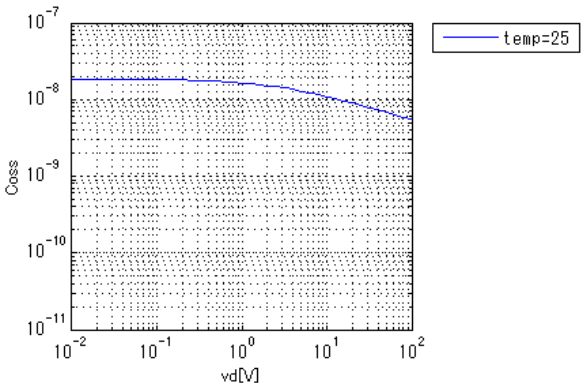
Freq. = 1MHz



Simulation results are following.
Explanatory notes — : simulated

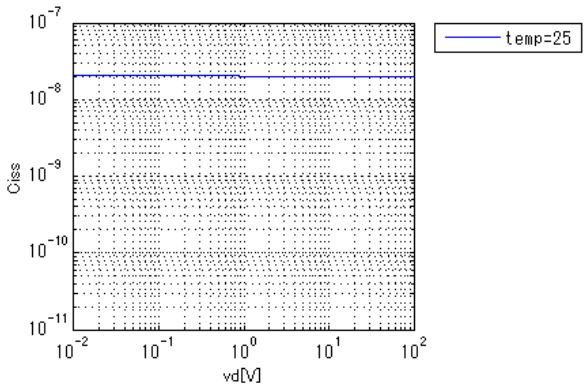
Coss

Freq. = 1MHz



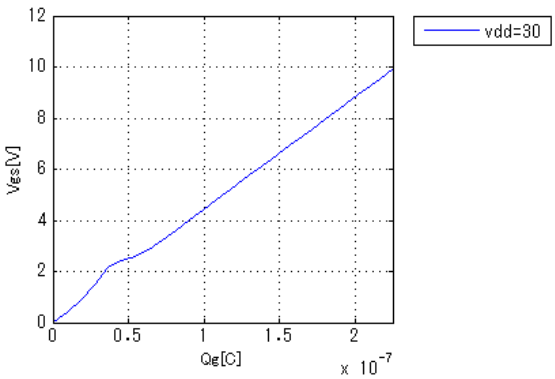
Ciss

Freq. = 1MHz

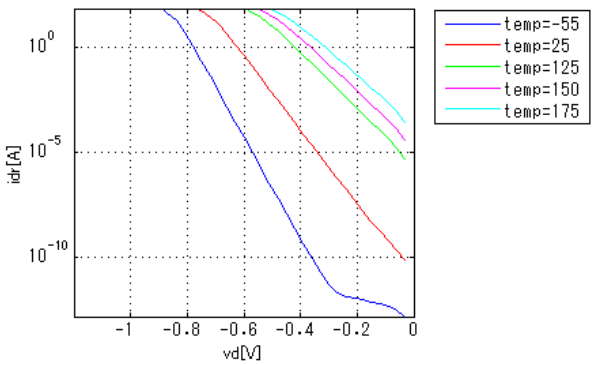


VgsQg[Vdd]

Id = 50A

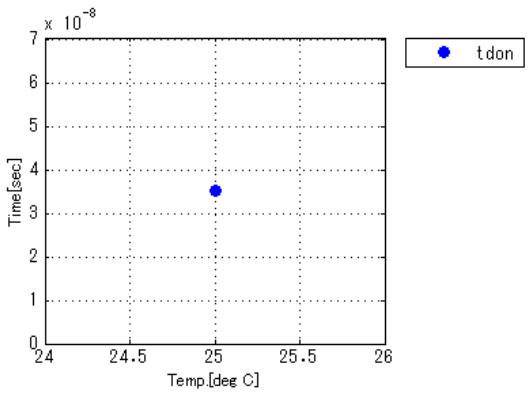


IsVsd[Temp]



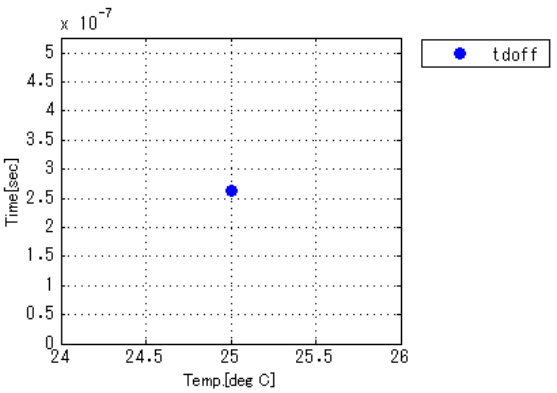
tdon

Vdd = 30V, Id = 50A, +Vg = 10V, -Vg = 0V, Rg = 2.5ohm



tdoff

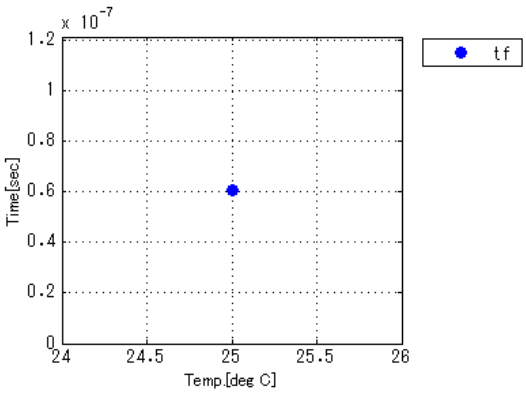
Vdd = 30V, Id = 50A, +Vg = 10V, -Vg = 0V, Rg = 2.5ohm



Simulation results are following.
Explanatory notes　— : simulated

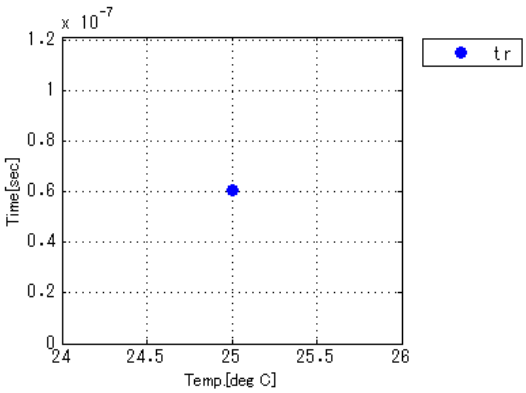
tf

Vdd = 30V, Id = 50A, +Vg = 10V, -Vg = 0V, Rg = 2.5ohm



tr

Vdd = 30V, Id = 50A, +Vg = 10V, -Vg = 0V, Rg = 2.5ohm



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