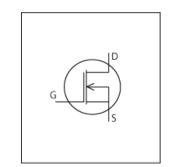


PSpice Model NMOS STM STB45N60DM2AG



Model Information

Model A macro model based on BSIM3
Call Name MDC_STB45N60DM2AG_PS

Pin Assign 1:D 2:G 3:S

File List Model Library MDC_STB45N60DM2AG_PS01.lib

Model Report MDC_STB45N60DM2AG_PS.pdf (this file)

Verified Simulator Version

Note

PSpice version 16.6

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version Rev 1

Product nameCompany nameSTB45N60DM2AGSTMicroelectronics N.V.

Characteristics IdVgs[Temp],IdVds[Vgs],Rds(on)Id[Vgs],VgsQg[Vdd],VdsQg[

Vdd], Ciss, Coss, Crss, Vth Temp[Id], Rds(on) Temp[Vgs], Is Vsd[

Temp]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

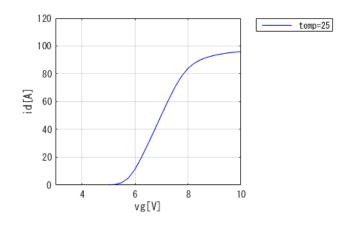
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	650	V
Gate-source voltage (DC)	0	to	25	V
Temperature	-55	to	150	deg C



Simulation results are following. Explanatory notes — : simulated

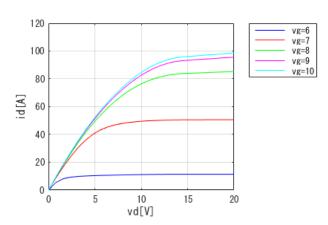
IdVgs[Temp]

Vds = 15V



IdVds[Vgs]

Temp. = 25deg C

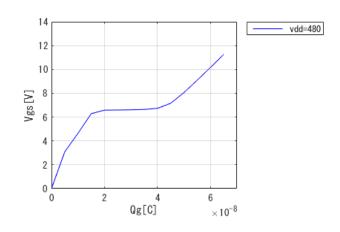


Rds(on)Id[Vgs]

0. 1 0. 095 0. 099 0. 085 0. 085 0. 085 0 id[A]

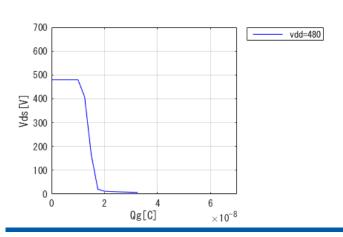
VgsQg[Vdd]

Id = 34A



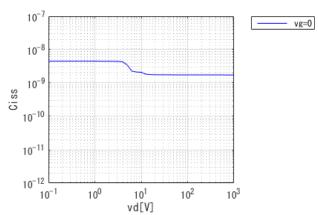
VdsQg[Vdd]

Id = 34A



Ciss

Freq. = 1MHz

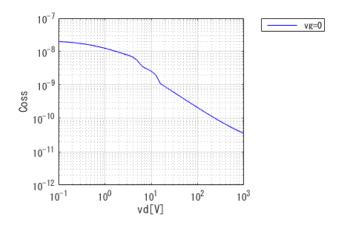




Simulation results are following. Explanatory notes — : simulated

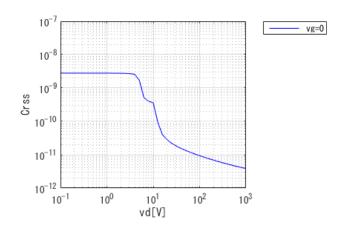
Coss

Freq. = 1MHz



Crss

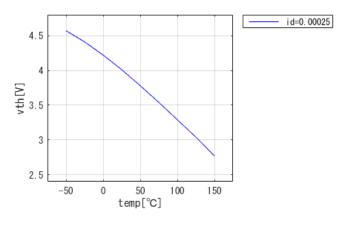
Freq. = 1MHz

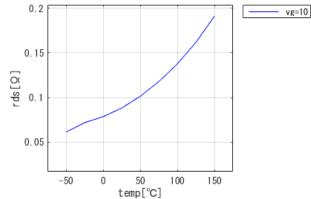


VthTemp[Id]

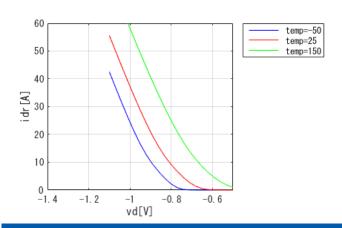
Rds(on)Temp[Vgs]

Id = 30A





IsVsd[Temp]





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