

PSpice Model

NMOS

RENESAS

UPA1764



Model Information

Model A macro model based on BSIM3
Call Name MDC_UPA1764_PS
Pin Assign 1:D 2:G 3:S
File List Model Library MDC_UPA1764_PS01.lib
 Model Report MDC_UPA1764_PS.pdf (this file)

Verified Simulator Version PSpice version 16.6
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version May-01
- Product name UPA1764
- Company name Renesas Electronics Corporation
- Characteristics IdVgs[Temp], IdVds[Vgs], Crss, Coss, Ciss, Rds(on)Vgs[Id], Rds(on)Id[Vgs], VthTemp[Id], Rds(on)Temp[Vgs], IsVsd[Vgs], VdsQg[Vdd], VgsQg[Vdd]

Simulation Range

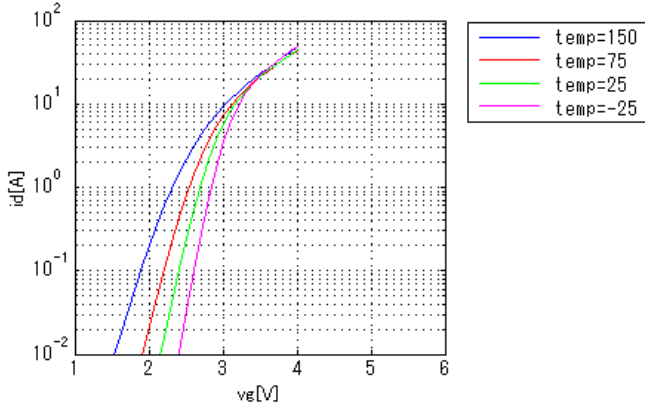
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	0	to	20	V
Temperature	-55	to	150	deg C

Simulation results are following.
 Explanatory notes — : simulated

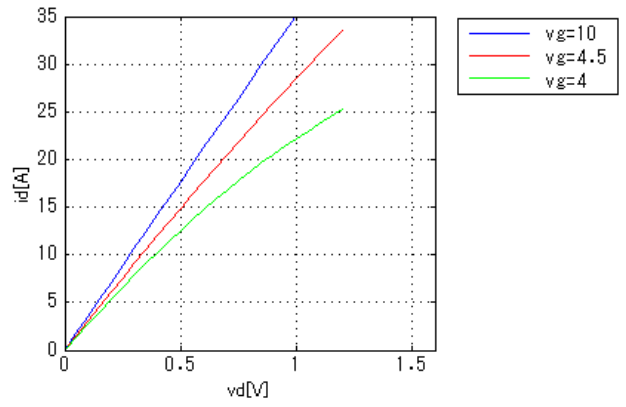
IdVgs[Temp]

Vds = 10V



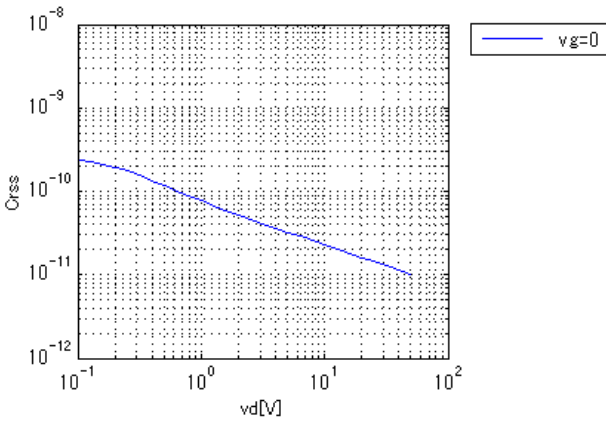
IdVds[Vgs]

Temp. = 25deg C



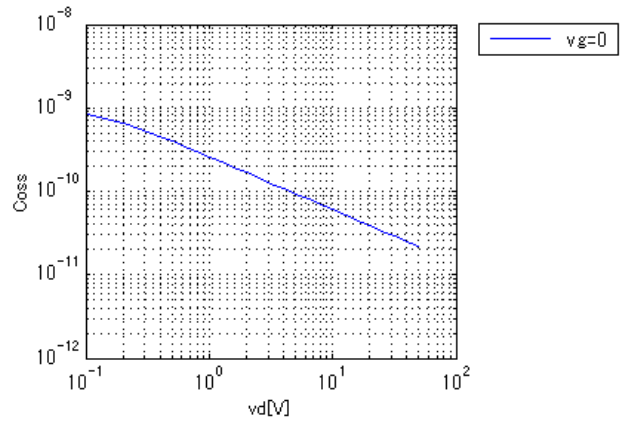
Crss

Freq. = 1MHz



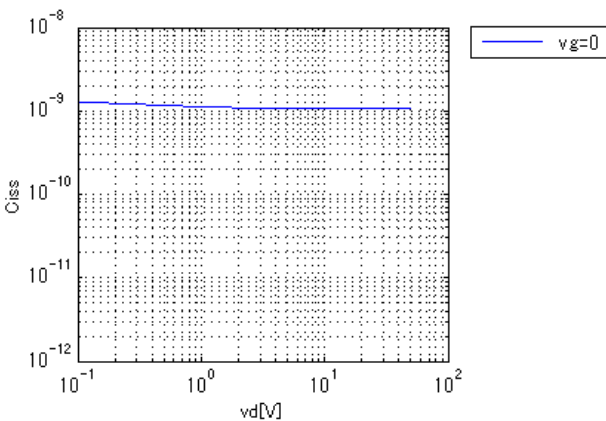
Coss

Freq. = 1MHz

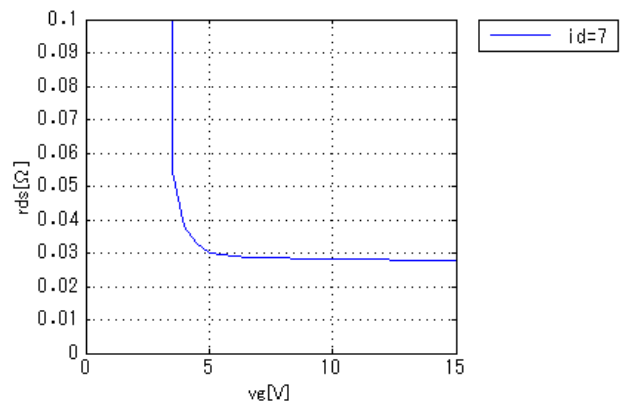


Ciss

Freq. = 1MHz

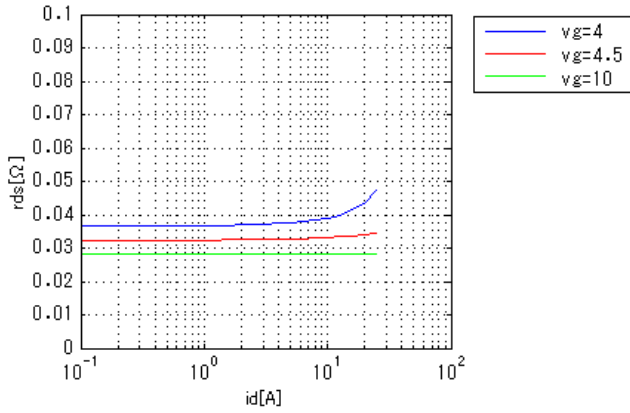


Rds(on)Vgs[Id]



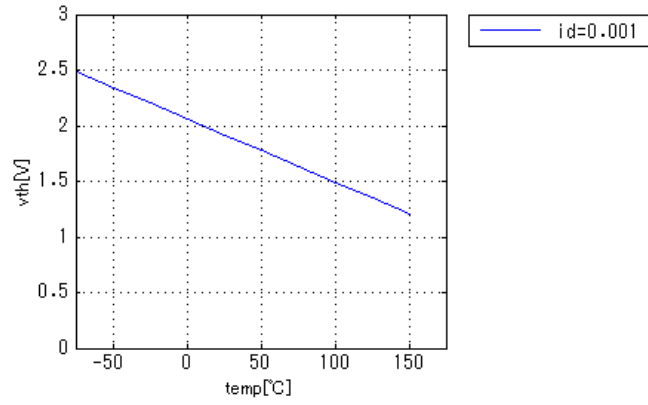
Simulation results are following.
 Explanatory notes — : simulated

Rds(on)Id[Vgs]



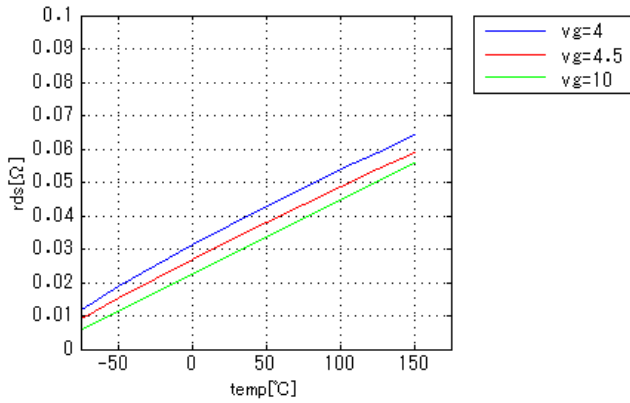
VthTemp[Id]

$V_{ds} = 10V$

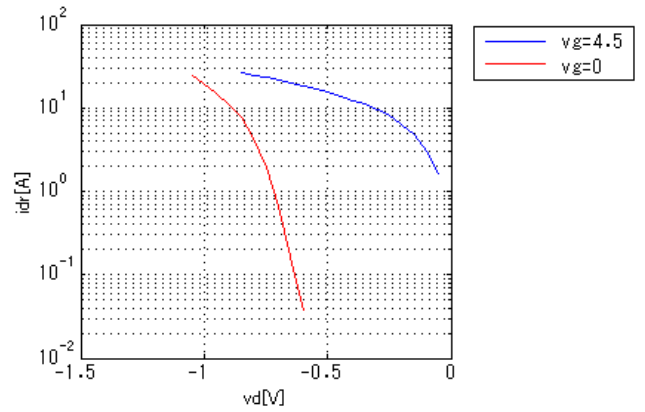


Rds(on)Temp[Vgs]

$I_d = 3.5A$

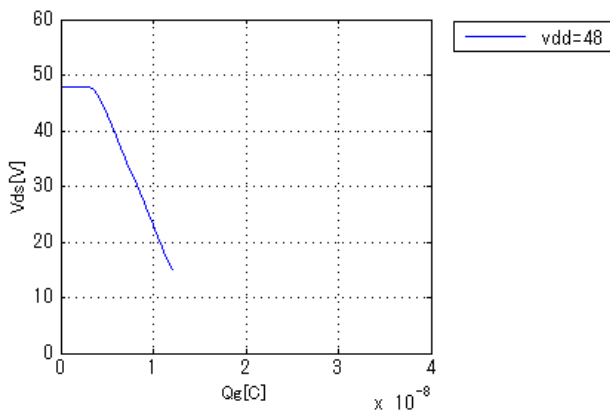


IsVsd[Vgs]



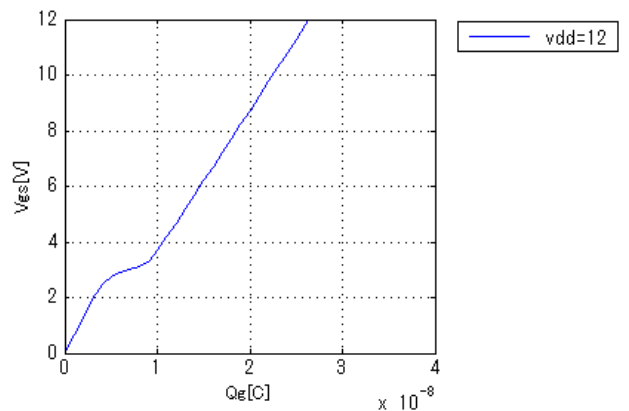
VdsQg[Vdd]

$I_d = 7A$



VgsQg[Vdd]

$I_d = 7A$



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