ADS Model
Operational Amplifier
Nisshinbo Micro Devices Inc.
NJM2904CG

Model Information

Model	A macro model
Call Name	MDC_NJM2904CG_AD
Pin Assign	1:AOUTPUT 2:A-INPUT 3:A+INPUT 4:V- 5:B+INPUT 6:B-INPUT 7:BOUTPUT 8:V+
File List	Model Library MDC_NJM2904CG_AD.lib
	Model Report MDC_NJM2904CG_AD.pdf(this file)

Verified Simulator Version ADS 2020 Update 2

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- ●Date/Version 2023.10.13 Ver.14
- ●Product name NJM2904C/NJM2904CA
- ●Company name Nisshinbo Micro Devices Inc.(NreJRC)

[Characteristics listed]

- ●Characteristics
  - Open Loop Gain
  - Input offset voltage
  - Input offset current
  - Input bias current
  - Output current limit
  - Slew Rate

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

○ : Implemented
× : Not Implemented
— : Not applicable

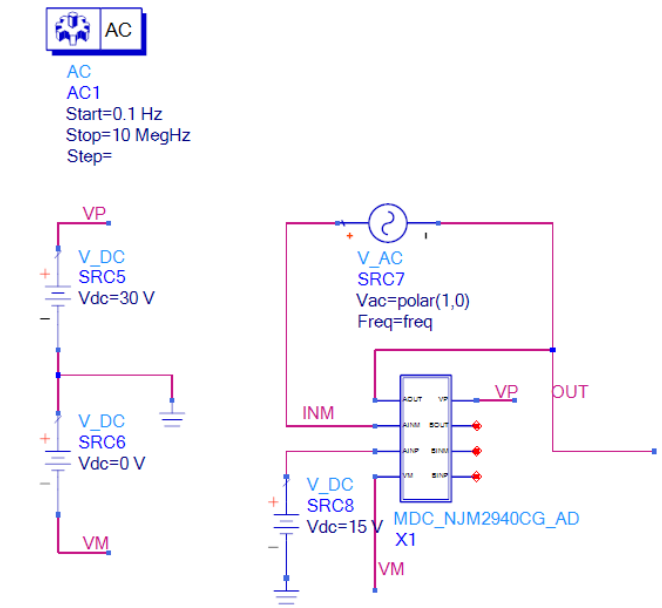
Model Functions Table

	RANK=1	
Functions	RANK	Implemented
Open Loop Gain	1	○
Unity Frequency	1	○
Phase Margin	1	—
Input Offset Voltage	1	○
Input Offset Current	1	○
Bias Current	1	○
Maximum output amplitude voltage	1	○
Slew Rate	1	○
Equivalent Input Noise Voltage	2	—
Equivalent Input Noise Current	2	—

Open Loop Gain

Simulation results are following.
Explanatory notes　— : simulated

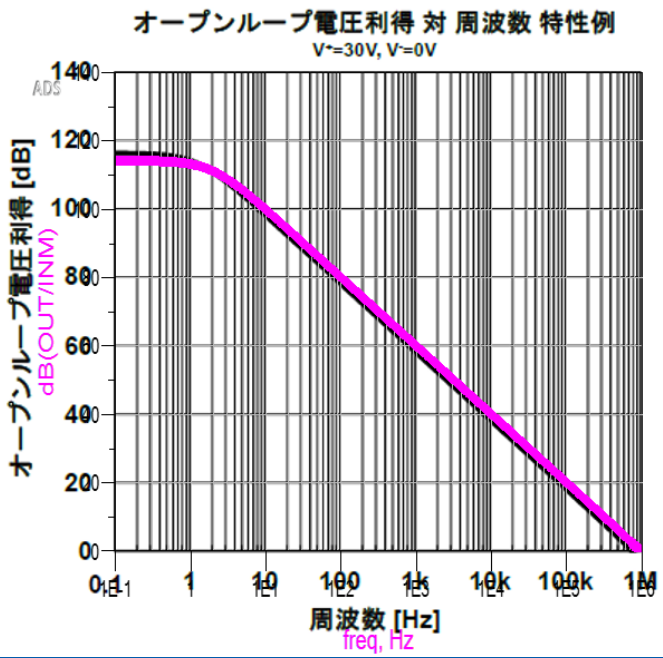
Testbench



Open Loop Gain

Simulation results are following.
Explanatory notes　— : simulated

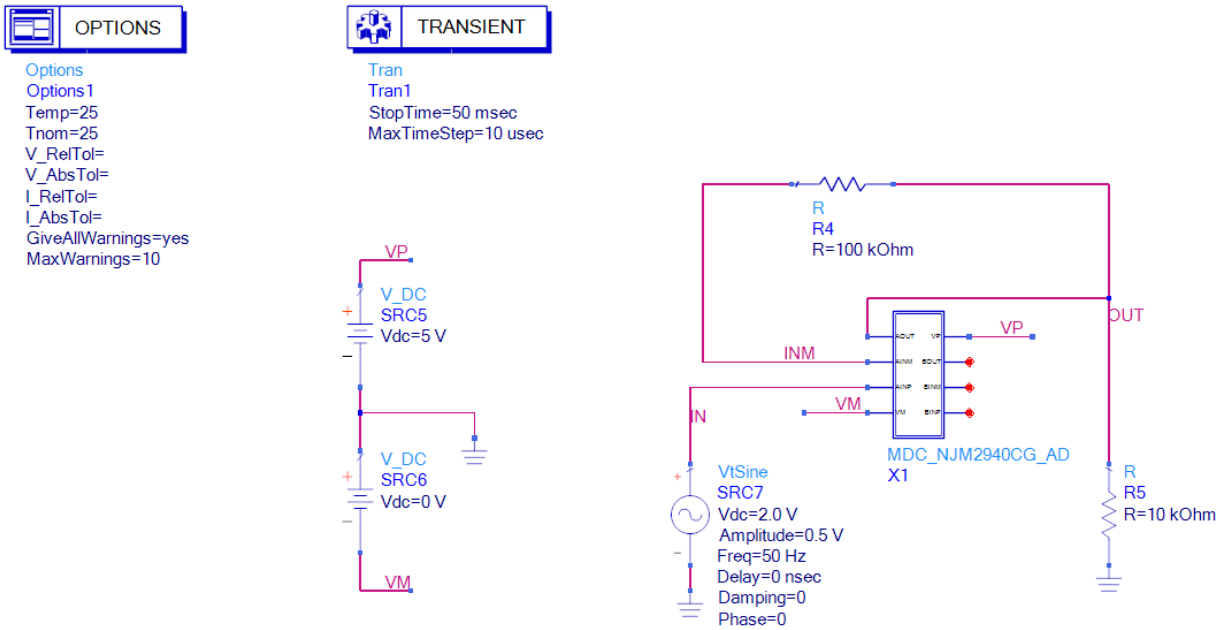
Sim result



Input offset voltage

Simulation results are following.
Explanatory notes — : simulated

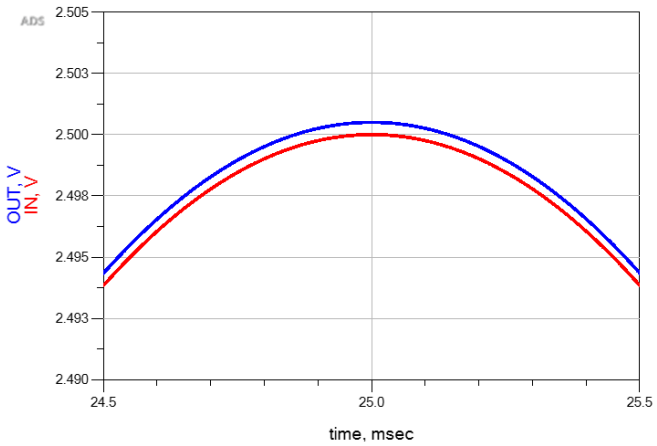
Testbench

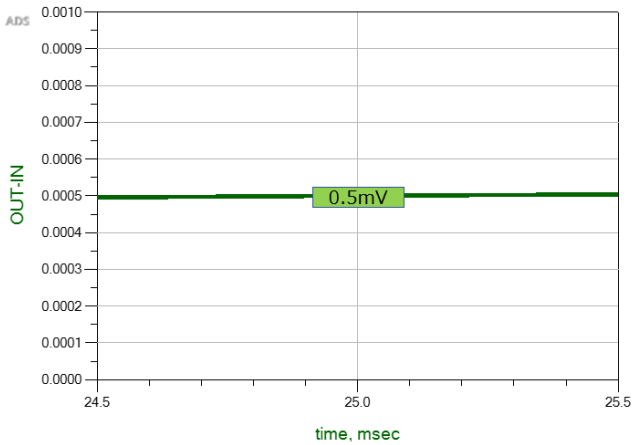


Input offset voltage

Simulation results are following.
Explanatory notes — : simulated

Sim result

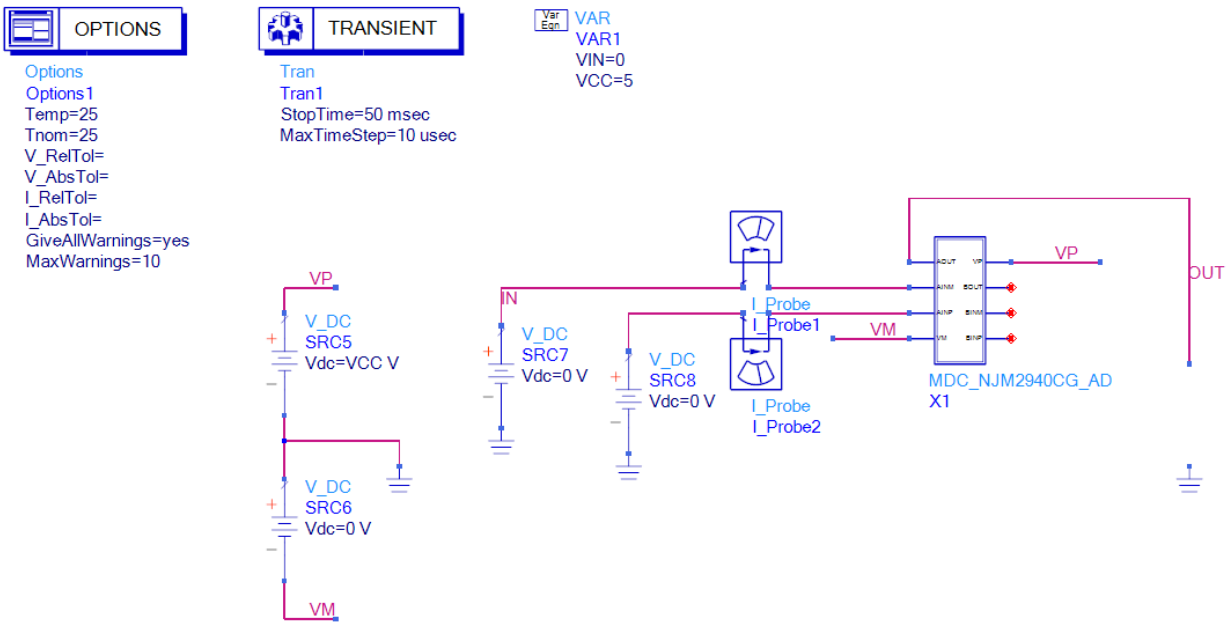




Input offset current

Simulation results are following.
Explanatory notes — : simulated

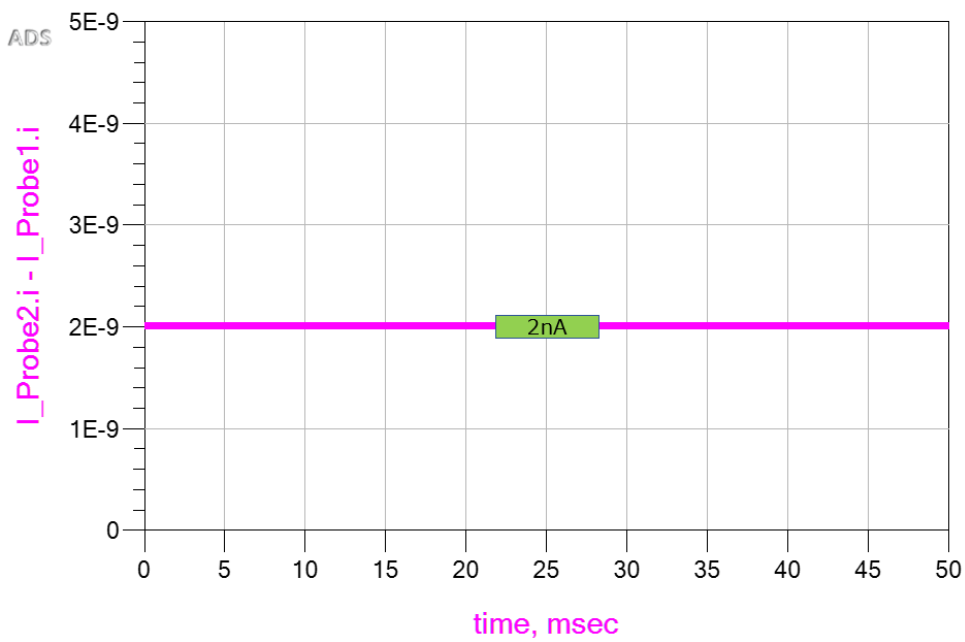
Testbench



Input offset current

Simulation results are following.
Explanatory notes — : simulated

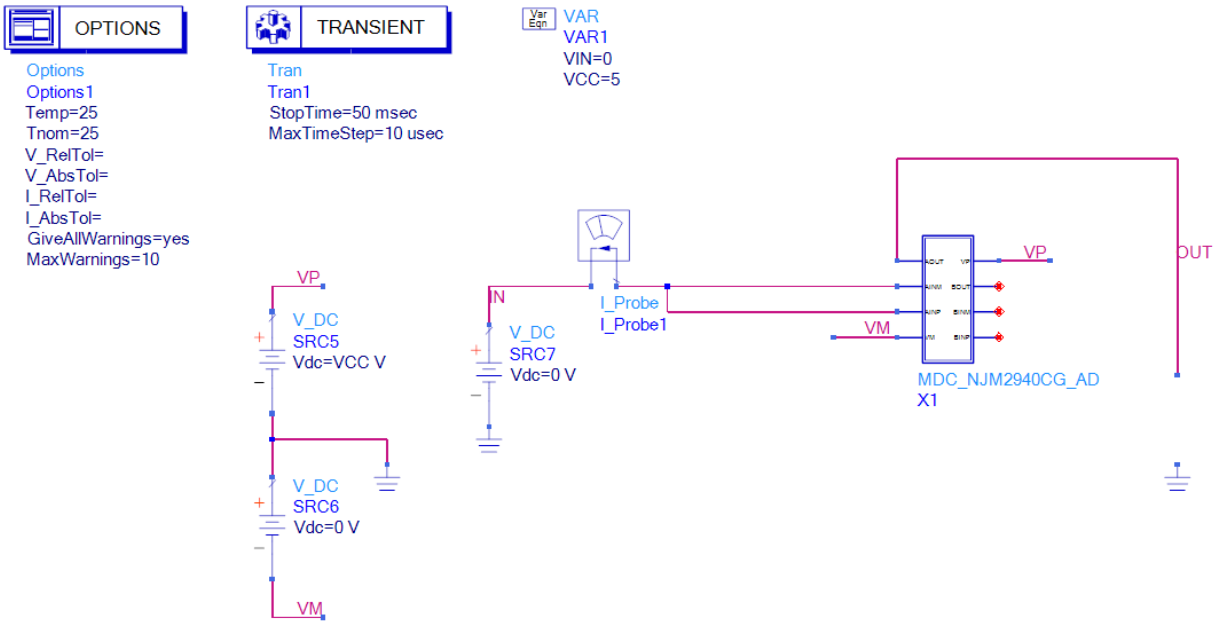
Sim result



Input bias current

Simulation results are following.
Explanatory notes — : simulated

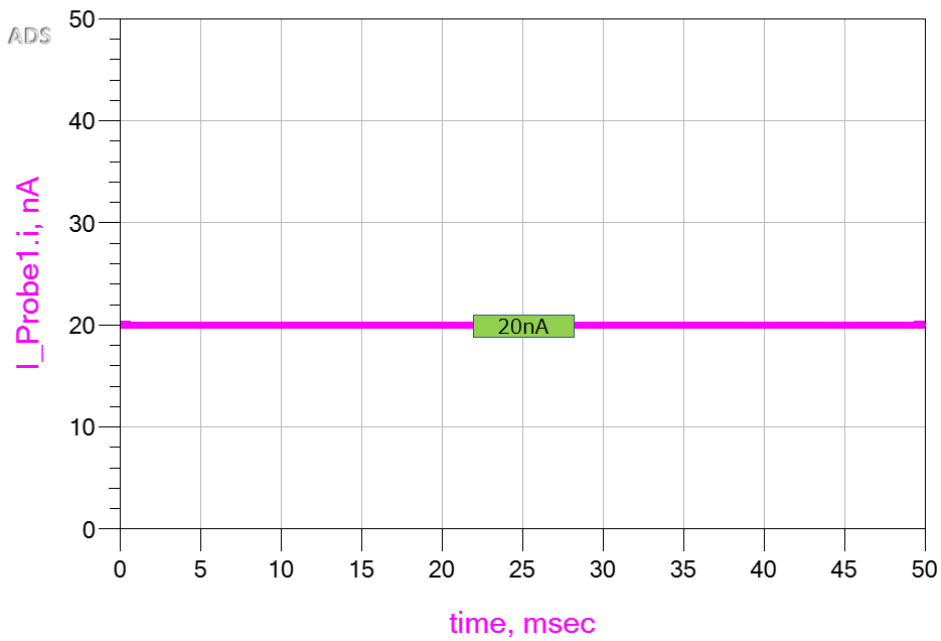
Testbench



Input bias current

Simulation results are following.
Explanatory notes — : simulated

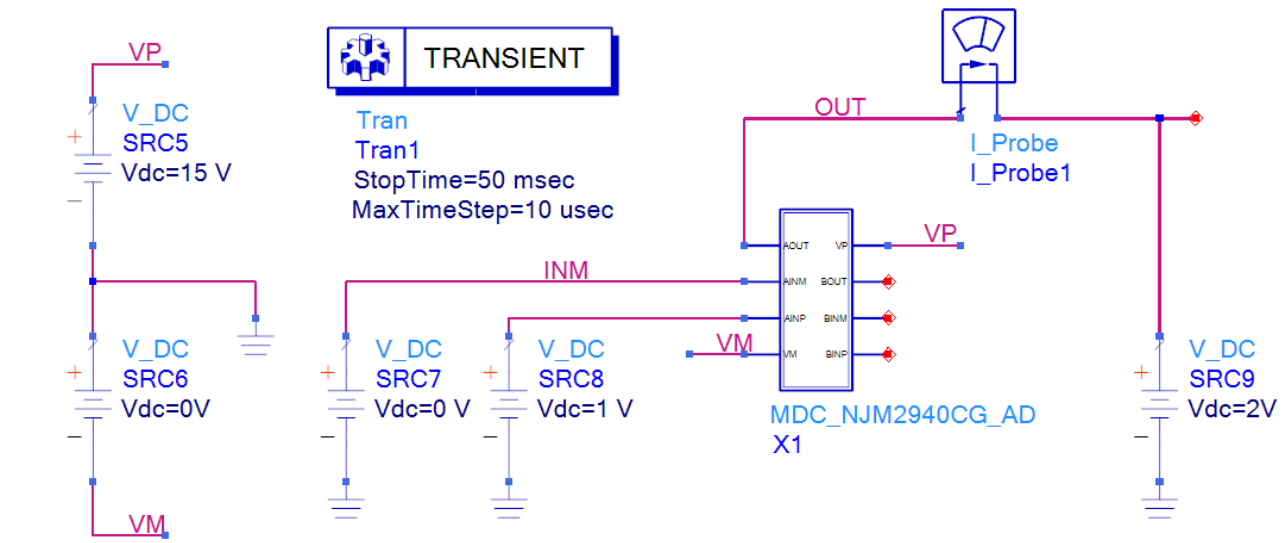
Sim result



Output current limit(Source Current)

Simulation results are following.
Explanatory notes — : simulated

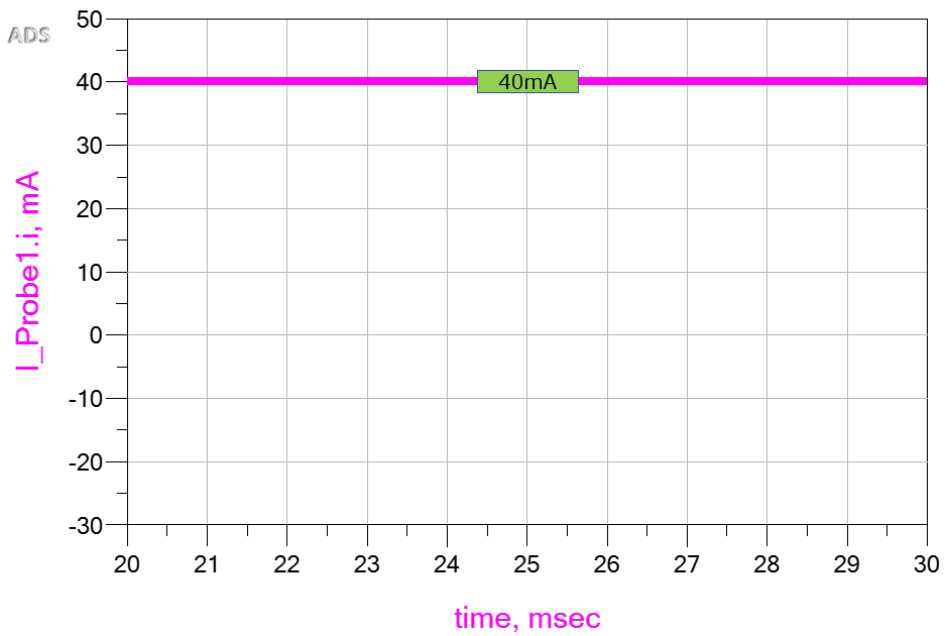
Testbench



Output current limit(Source Current)

Simulation results are following.
Explanatory notes — : simulated

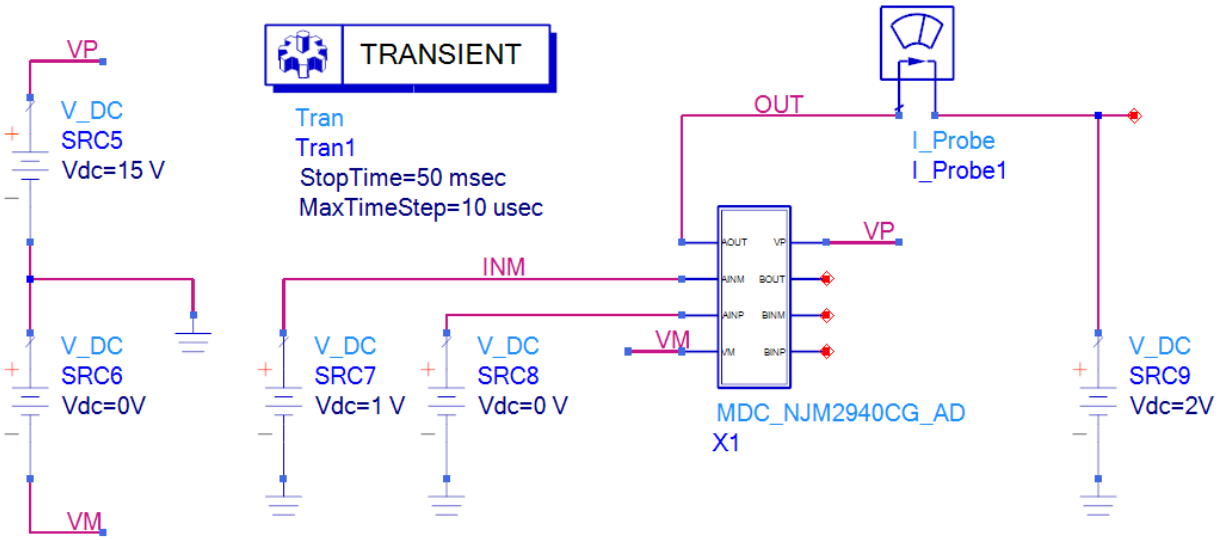
Sim result



Output current limit(Sink Current)

Simulation results are following.
Explanatory notes — : simulated

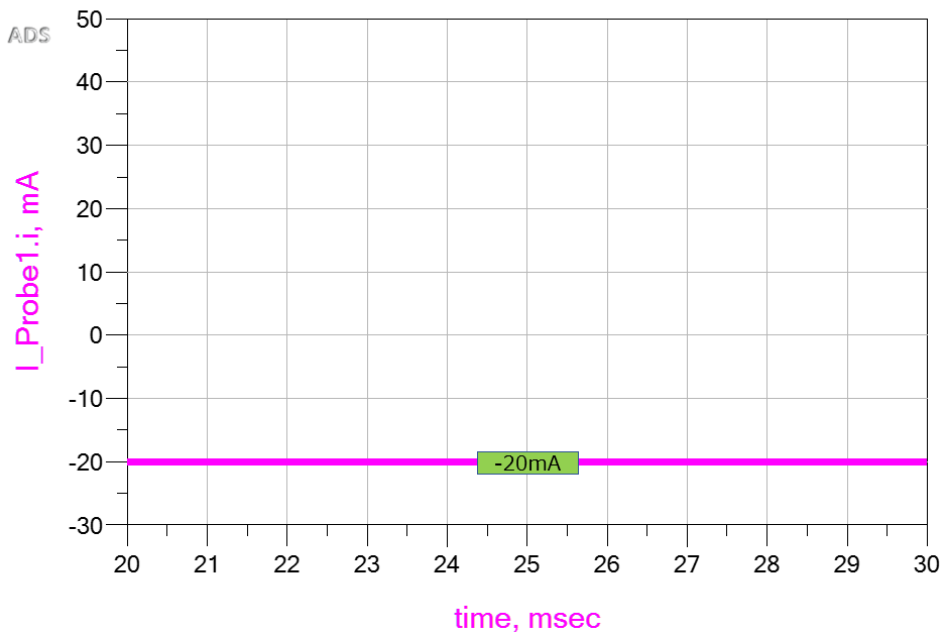
Testbench



Output current limit(Sink Current)

Simulation results are following.
Explanatory notes — : simulated

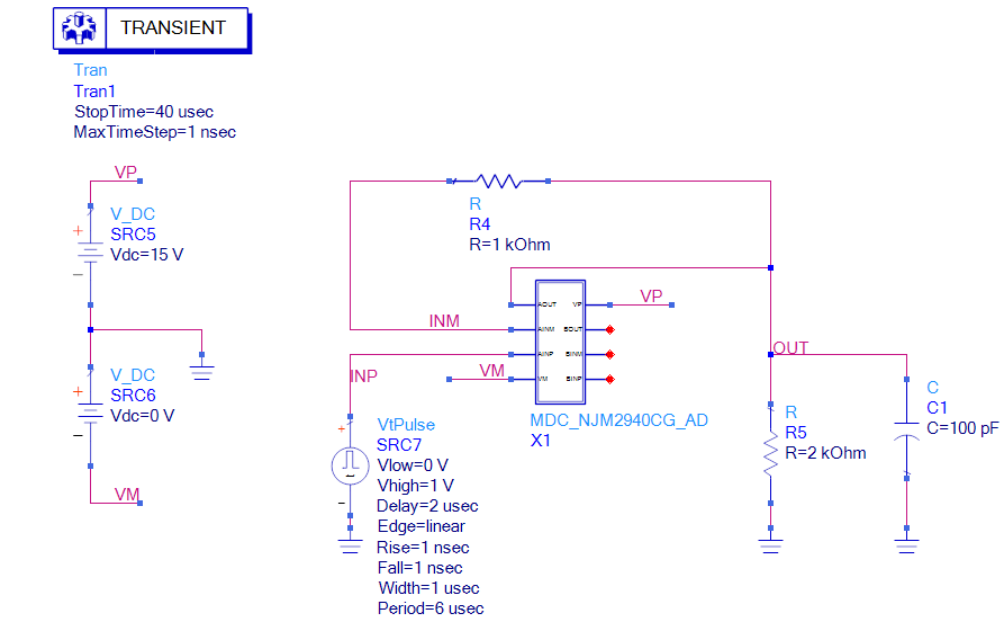
Sim result



Slew Rate

Simulation results are following.
Explanatory notes — : simulated

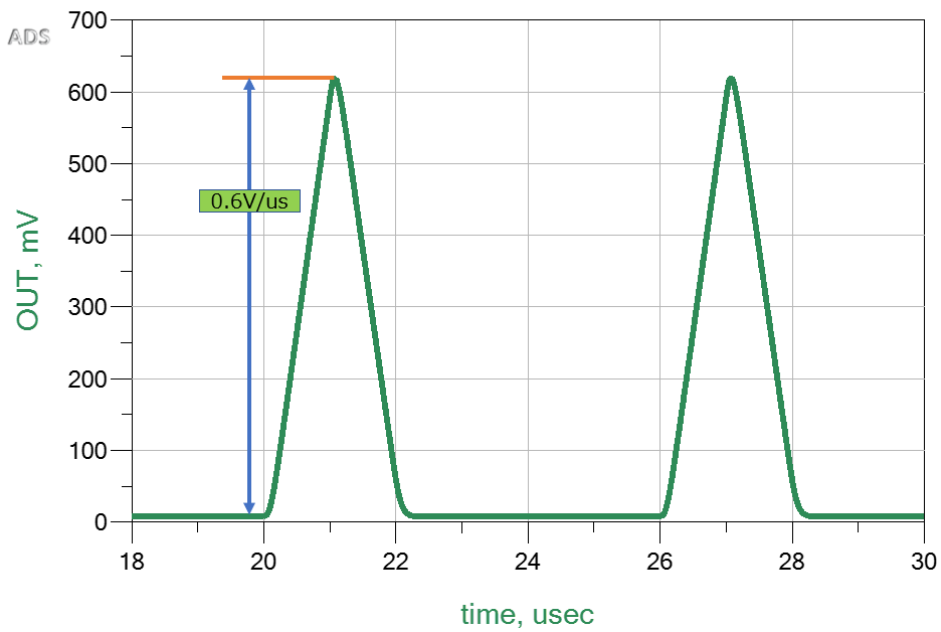
Testbench



Slew Rate

Simulation results are following.
Explanatory notes — : simulated

Sim result



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