

PSpice Model

N-Channel JFET

TOSHIBA

2SK208

Model Information

Model A macro model
Call Name MDC_2SK208_PS
Pin Assign 1:S 2:D 3:G
File List Model Library MDC_2SK208_PS.lib
 Model Report MDC_2SK208_PS.pdf

Verified Simulator Version

Note

IDSS=2.6~6.5mA(GR)

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 1 Mar 2014
- Product name 2SK208
- Company name TOSHIBA

[Characteristics listed]

- Characteristics IdVgs[Temp],IdVds[Vgs],VGS(off),yfs-IDSS, Crs,Cis

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

JFET

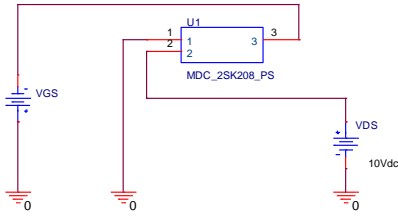
○ : Implemented
 × : Not Implemented
 — : Not applicable

Model Functions Table
RANK=1

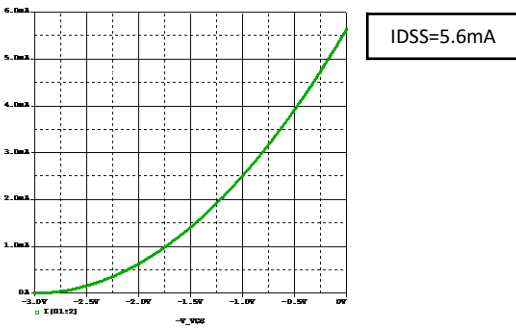
Functions	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS	1	○
VGS(off)-IDSS	1	○
yfs-IDSS	1	○
RDS(on)-IDSS	1	—
Crs Capacitance	1	○
Cis Capacitance	1	○

Simulation results are following.
 Explanatory notes — : simulated

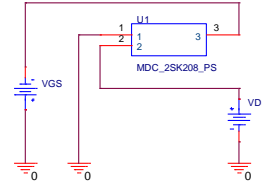
IdVgs[Temp] Testbench



IdVgs[Temp] Data Sheet

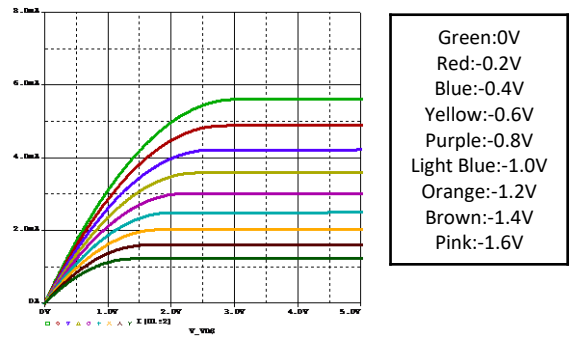


IdVds[Vgs] Testbench



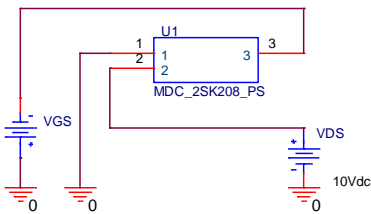
IdVds[Vgs] Data sheet

Characteristics of Id-Vgs are prioritized.



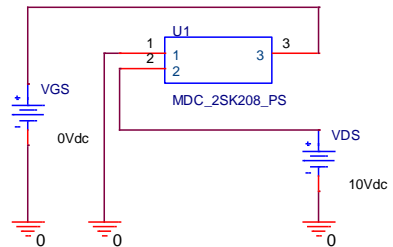
VGS(off) Testbench

CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vds = 10 V, Id = 0.1 μA	-0.4	-	-5.0	V

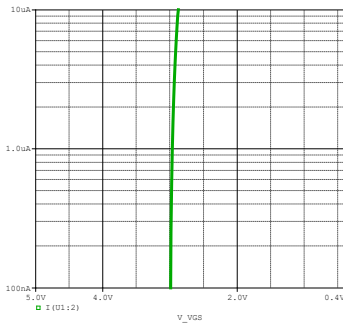


yfs-IDSS Testbench

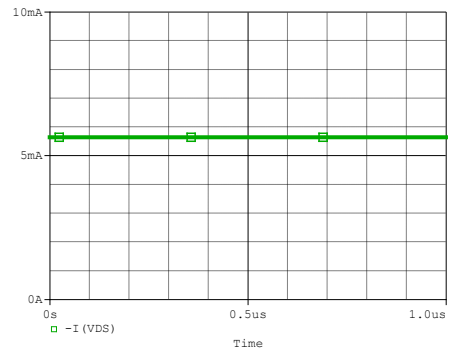
CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vds = 10 V, Vgs = 0	0.3	-	6.5	mA



VGS(off) Data Sheet



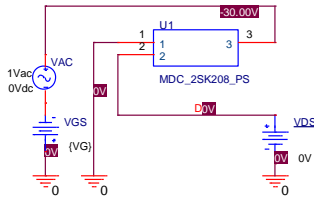
yfs-IDSS Data Sheet



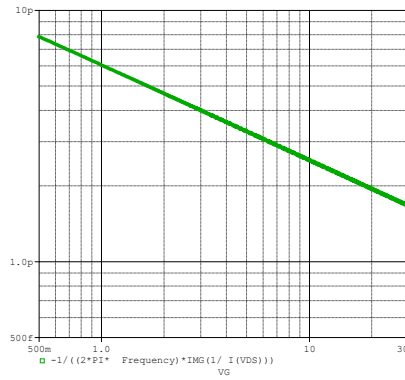
Simulation results are following.
 Explanatory notes — : simulated

Crs Capacitance Testbench

CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vgd = -10 V, Id = 0, f = 1MHz	-	8.2	-	pF



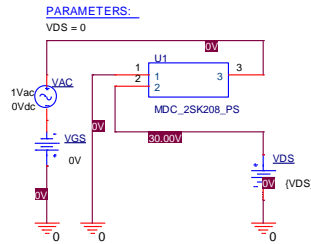
Crs Capacitance Data Sheet



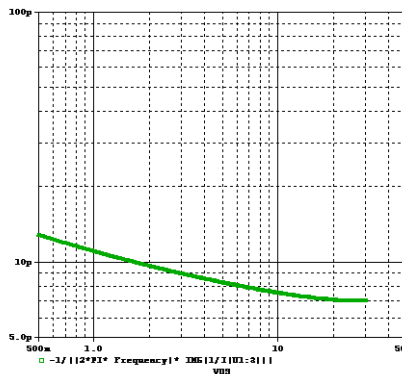
ID=0
 f=1MHz
 Ta=25°C

Cis Capacitance Testbench

CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vds = 10 V, Vgs = 0, f = 1MHz	-	8.2	-	pF



Cis Capacitance Data Sheet



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