LTspice Model
Logic IC
TI
CD4052BNSR

Model Information

Model	An original macro model
Call Name	MDC_CD4052BNSR_LT
Pin Assign	1:Ch_Y0 2:Ch_Y2 3:Y_com 4:Ch_Y3 5:Ch_Y1 6:INH 7:VEE 8:VSS 9:B 10:A 11:Ch_X3 12:Ch_X0 13:X_com 14:Ch_X1 15:Ch_X2 16:VDD
File List	Model Library MDC_CD4052BNSR_LT01.lib
	Model Report MDC_CD4052BNSR_LT.pdf (this file)

Verified Simulator Version	LTspice version XVII
Note	

References

The information which was used for modeling is as follow:

[Data Sheet]

●Date/Version	Unknown
●Product name	CD4052BNSR
●Company name	Texas Instruments Inc.
●Characteristics	X-Func-IN,X-Func-OUT,Y-Func-IN,Y-Func-OUT, Signal Input to Output,Address-to-Signal OUT, Inhibit-to-Signal OUT Turning ON, Inhibit-to-Signal OUT Turning OFF

Simulation Condition

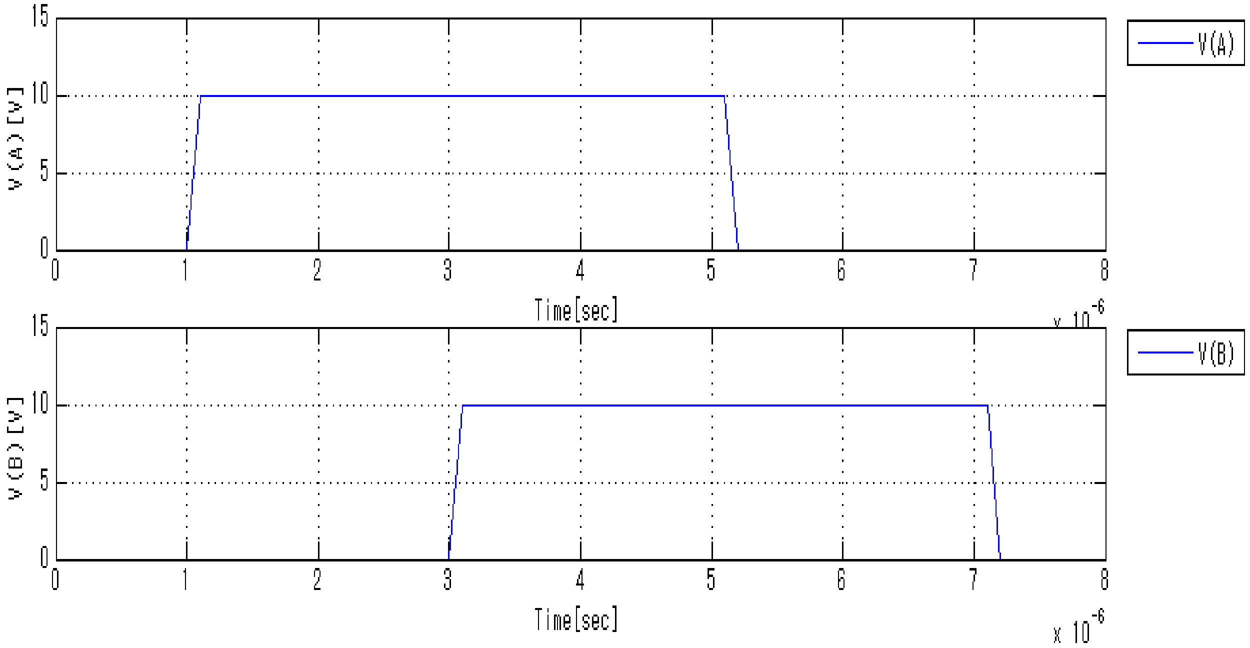
This table shows the value of evaluated simulation condition that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

Simulation results are following.
Explanatory notes — : simulated

X-Func-AddressIN

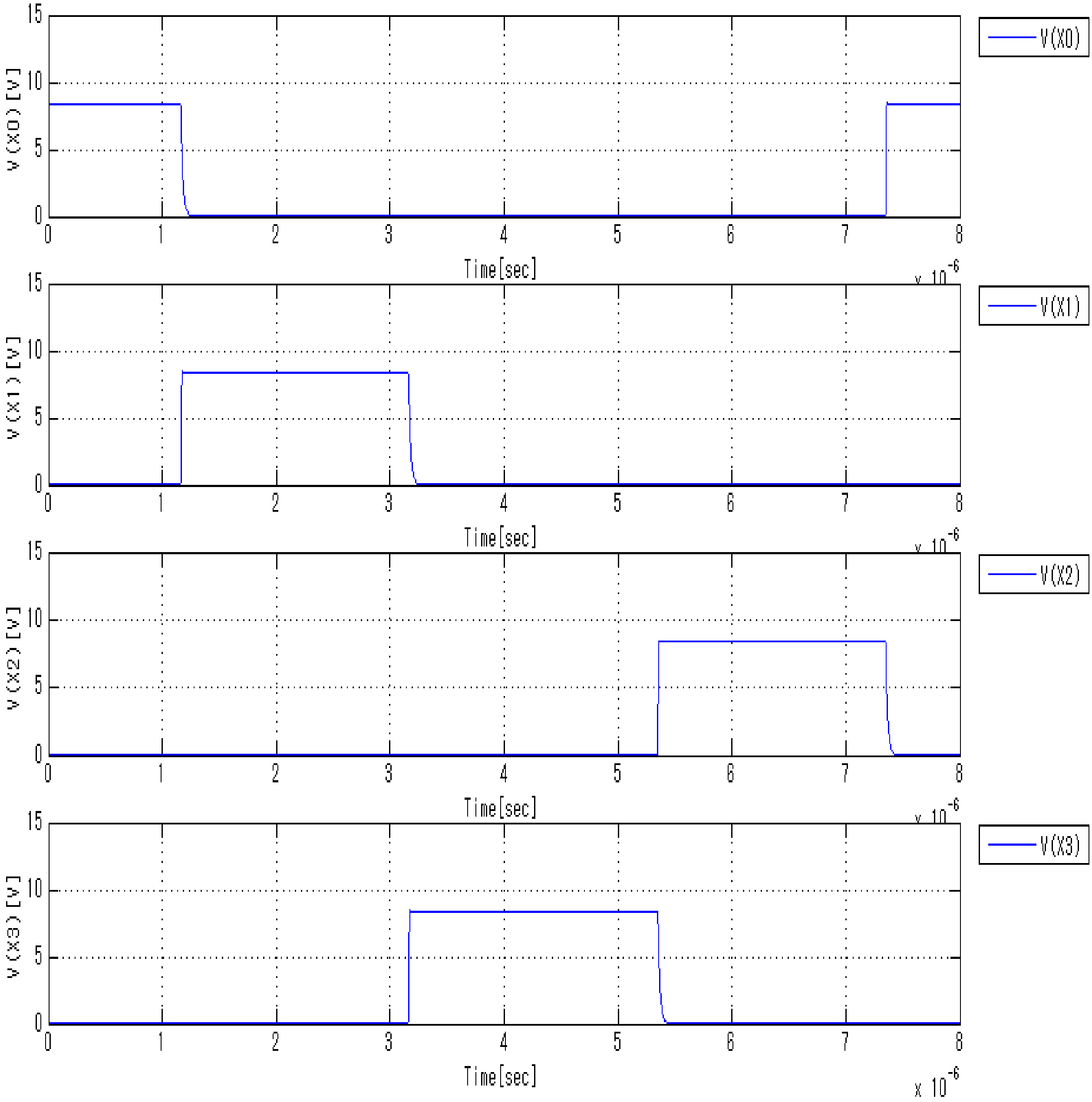
Temp. = 25deg C XCOM=10 V



Simulation results are following.
Explanatory notes — : simulated

X-Func-OUT

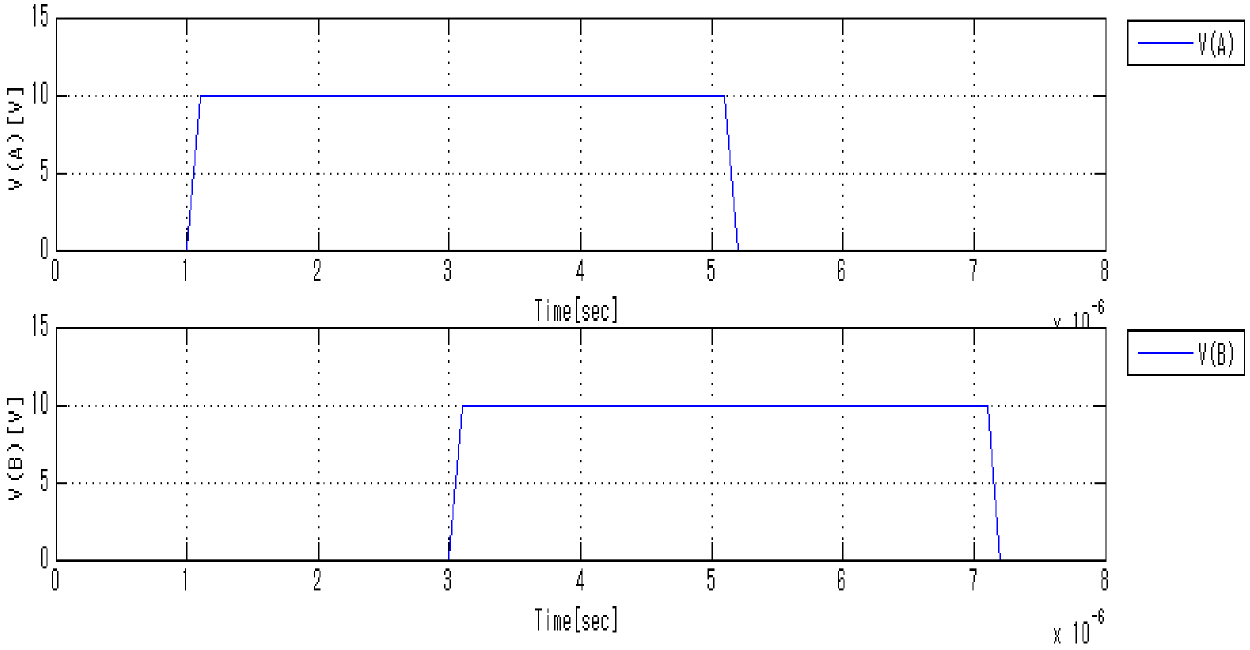
Temp. = 25deg C XCOM=10 V



Simulation results are following.
Explanatory notes　— : simulated

Y-Func-AddressIN

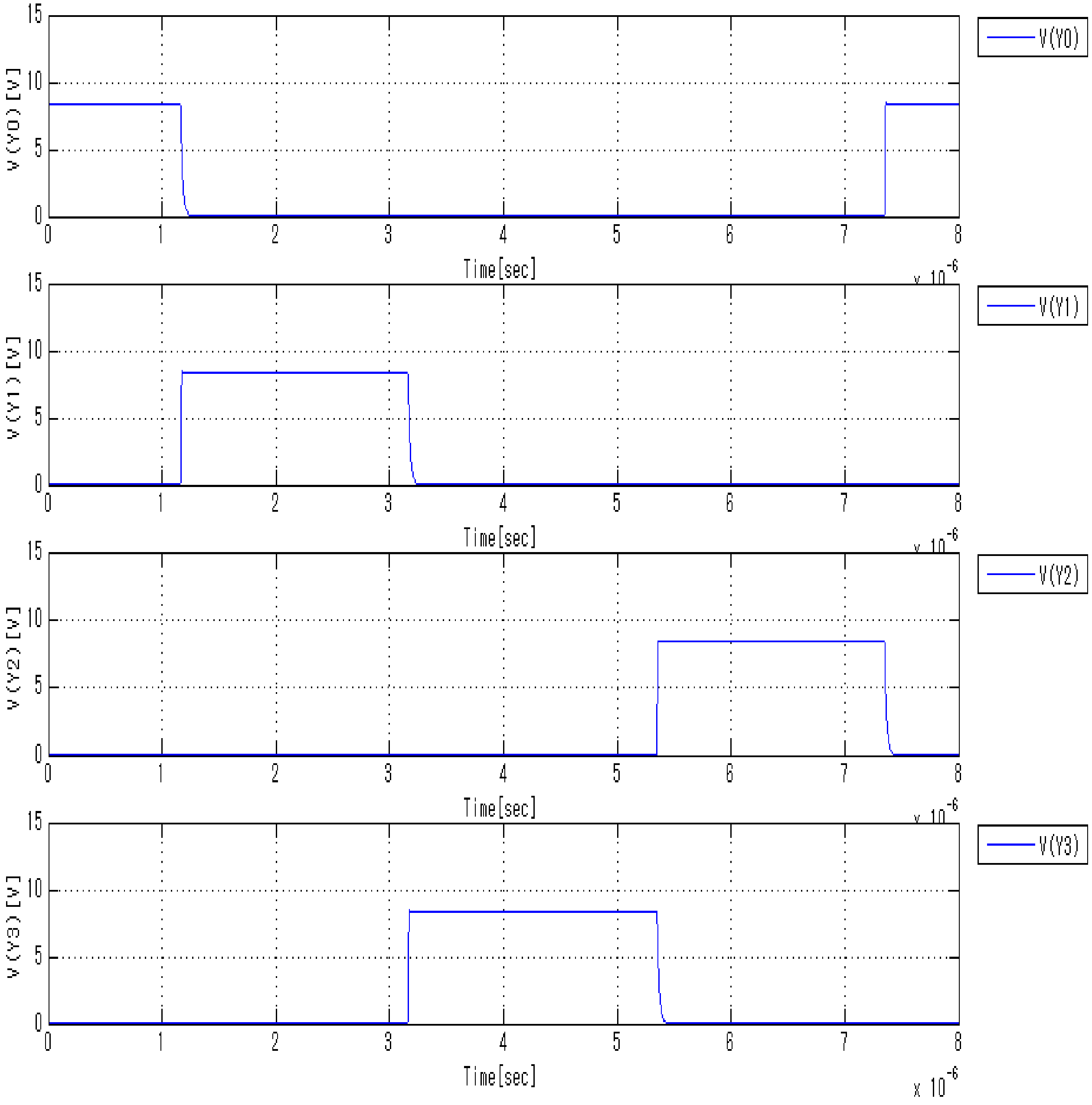
Temp. = 25deg C　YCOM=10 V



Simulation results are following.
Explanatory notes — : simulated

Y-Func-OUT

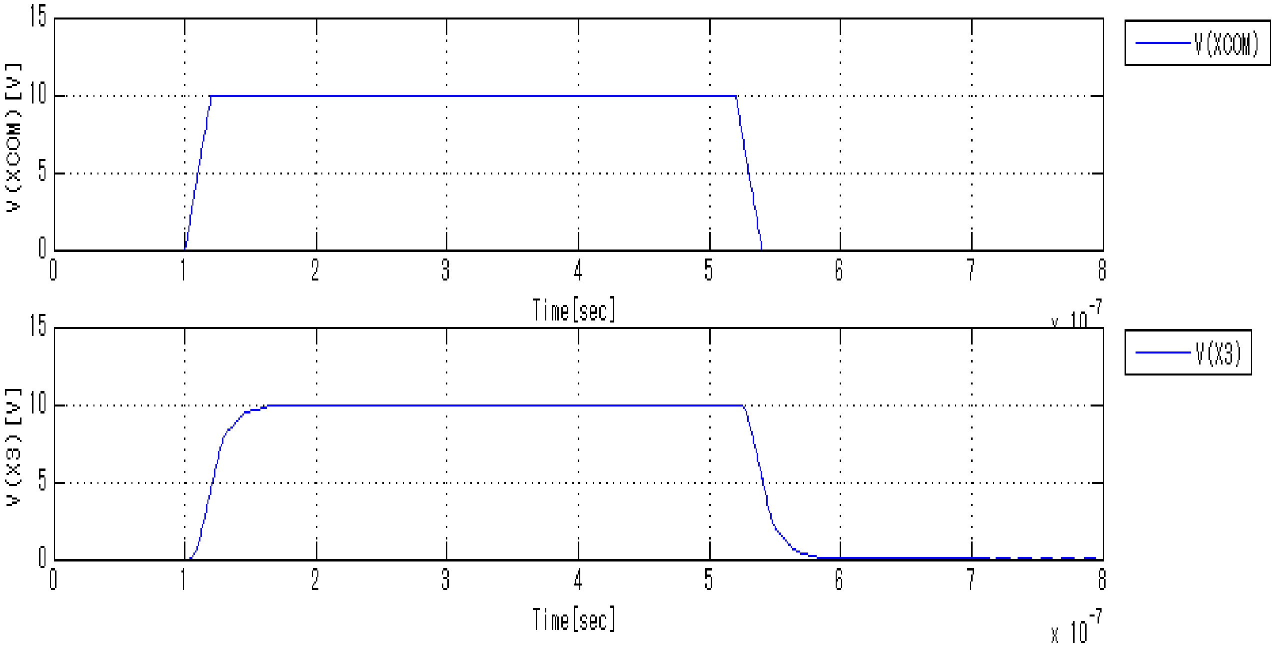
Temp. = 25deg C YCOM=10 V



Simulation results are following.
Explanatory notes — : simulated

Signal Input to Output

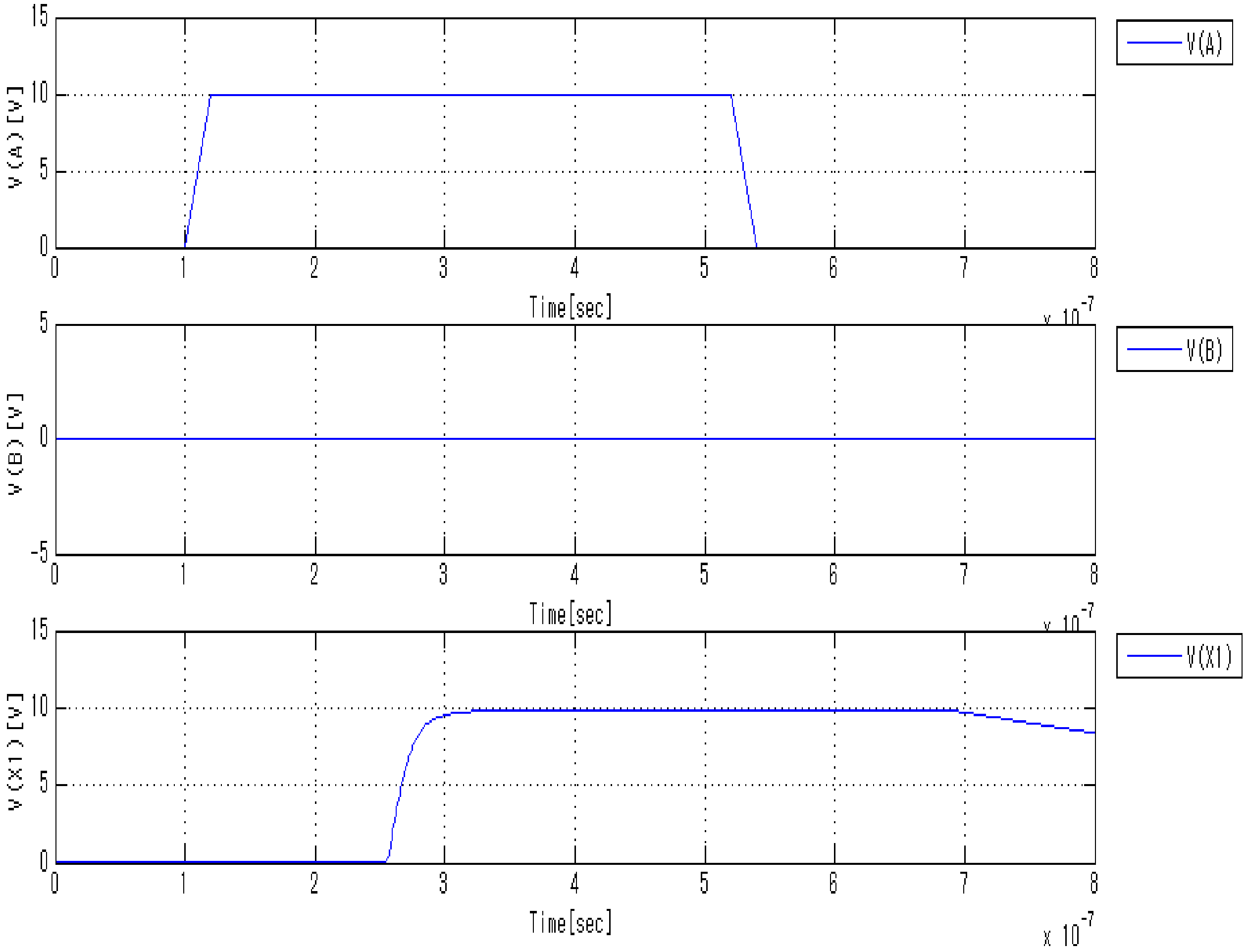
Temp. = 25deg C



Simulation results are following.
Explanatory notes — : simulated

Address-to-Signal OUT

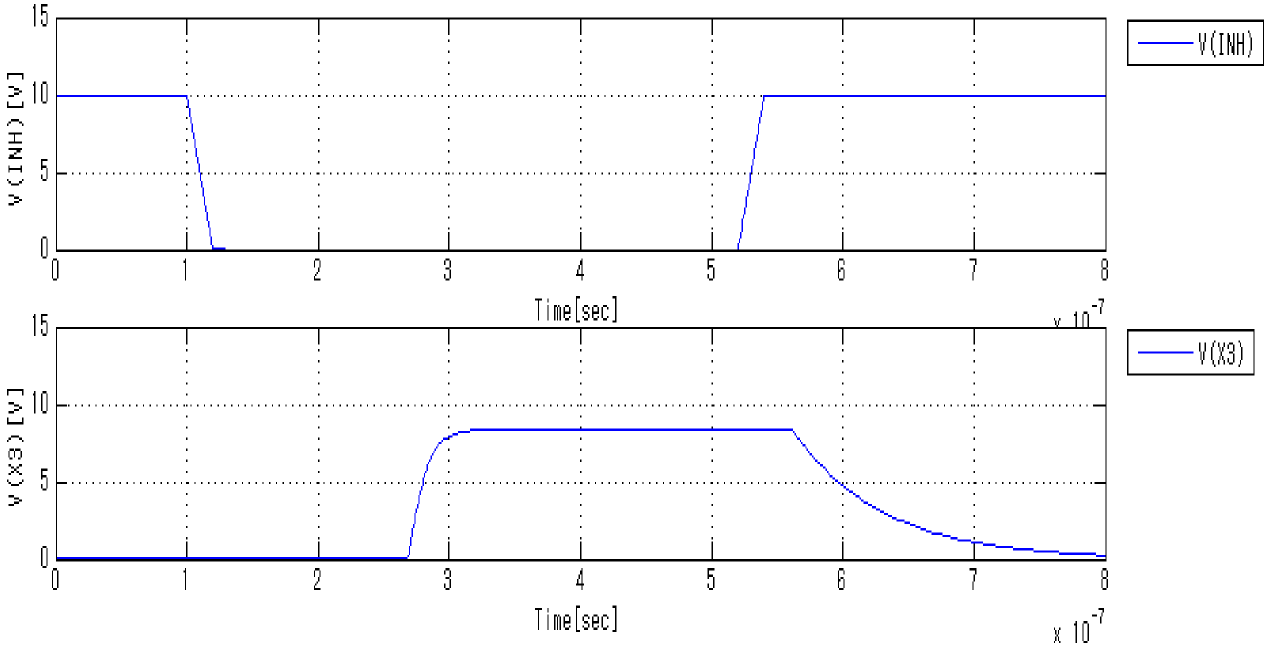
Temp. = 25deg C



Simulation results are following.
Explanatory notes — : simulated

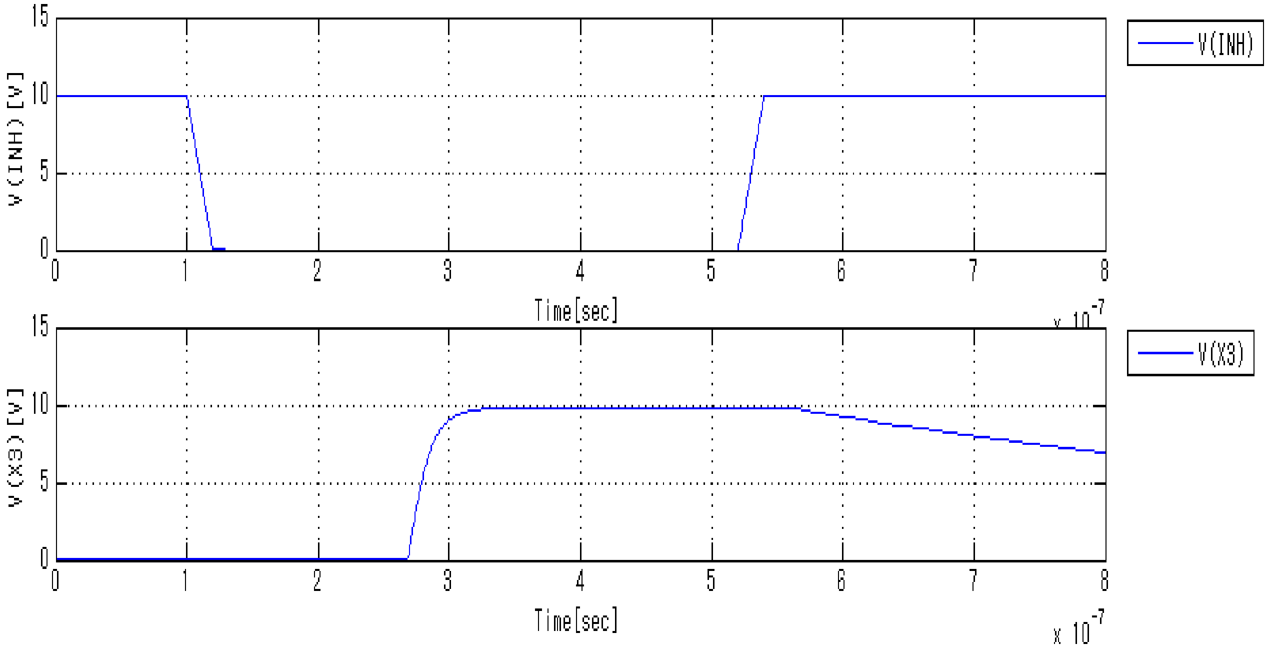
Inhibit-to-Signal OUT Turning ON

Temp. = 25deg C



Inhibit-to-Signal OUT Turning OFF

Temp. = 25deg C



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