

MDC_RJK0305DPB-02_PS

PSpice Model NMOS RENESAS RJK0305DPB-02

Model Information

G

 Model
 A macro model based on BSIM3 model

 Call Name
 MDC_RJK0305DPB-02_PS

 Pin Assign
 1:D 2:G 3:S

 File List
 Model Library
 MDC_RJK0305DPB-02_PS01.lib

 Model Report
 MDC_RJK0305DPB-02_PS.pdf (this file)

Verified Simulator Version Note

PSpice version 16.6

References

The information which was used for modeling is as follow:

[Data Sheet]
Date/Version
Product name
Company name
Characteristics

Rev.9.01 RJK0305DPB-02 Renesas Electronics Corporation IdVgs[Temp],IdVds[Vgs],Rds(on)Id[Vgs],Crss,Coss,Ciss,Vgs Qg[Vdd],VdsVgs[Id],Rds(on)Temp[Id],VdsQg[Vdd],IsVsd[Vgs]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

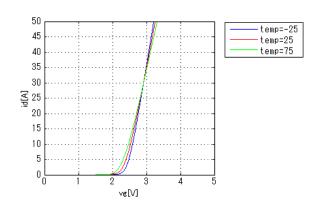
Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	30	V
Gate-source voltage (DC)	0	to	16	V
Temperature	-55	to	150	deg C



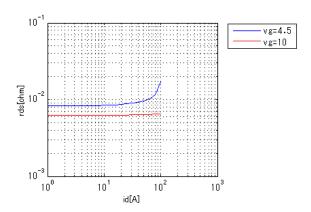
Simulation results are following. Explanatory notes — : simulated

IdVgs[Temp]

Vds = 10V

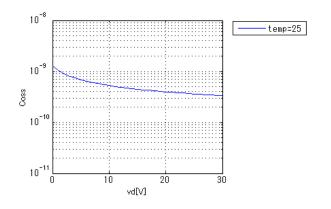


Rds(on)Id[Vgs]





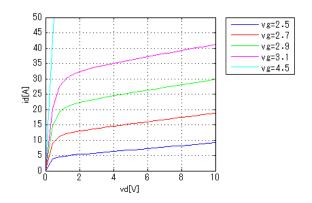
Freq. = 1MHz



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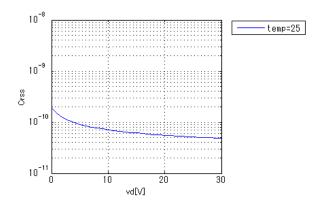
ldVds[Vgs]

Temp. = 25deg C

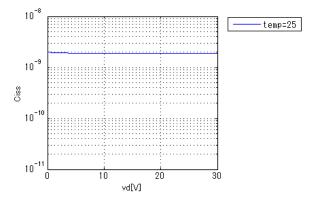




Freq. = 1MHz



Ciss Freq. = 1MHz

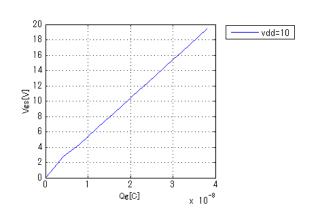




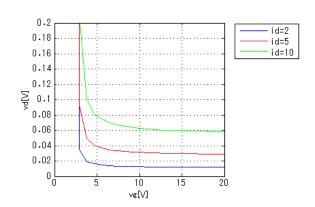
Simulation results are following. Explanatory notes — : simulated

VgsQg[Vdd]

Id = 30A

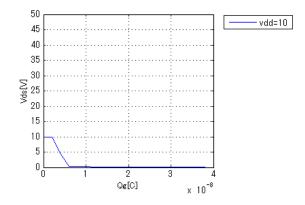


VdsVgs[ld]



VdsQg[Vdd]

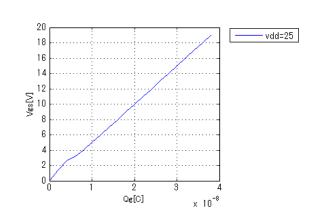
Id = 30A



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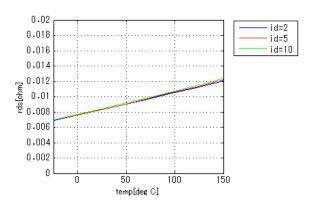
VgsQg[Vdd]

Id = 30A



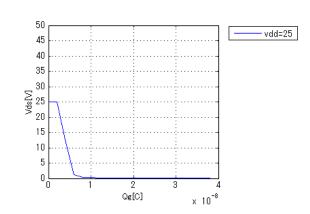
Rds(on)Temp[Id]

Vgs = 4.5V



VdsQg[Vdd]

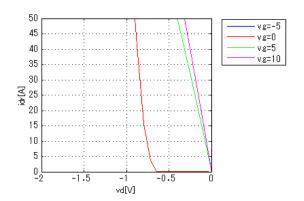
Id = 30A





Simulation results are following. Explanatory notes -: simulated

lsVsd[Vgs]





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MoDeCH Inc.

Head Office Location: Mitsuiseimei Hachioji Bldg., 5-15 Yokoyama-cho, Hachioji-Shi, Tokyo 192-0081, Japan Tel:+81-42-656-3360 E-Mail:model-on-support@modech.co.jp URL:http://www.modech.com/en/