LTspice Model
Forward/Reverse H-bridge Driver
ON Semiconductor
LV8760T-TLM-E

Model Information

Model	A macro model
Call Name	MDC_LV8760T-TLM-E_LT
Pin Assign	1:PGND 2,3:OUTB 4,5:RNF 6,7:VM 8,9:OUTA 10:PS 11:GND 12:VG 13:CP2 14:CP1 15:REG5 16:IN1 17:IN2 18:VREF 19:SCP VCC
File List	Model Library MDC_LV8760T-TLM-E_LT02.lib
	Model Report MDC_LV8760T-TLM-E_LT.pdf(this file)

Verified Simulator Version   LTspice XVII

Note

References
The information which was used for modeling is as follow:

[Data Sheet]
- ●Date/Version   August, 2013
- ●Product name   LV8760T-TLM-E
- ●Company name   ON Semiconductor

[Characteristics listed]
- ●Characteristics   VREG, VthVCC, VthHIS
  Ron1, Ron2, I0leak, tr, tf, tpLH, tpHL,
  VGH, tONG, Fcp, IINL, IINH, VINH, VINH,
  IREF, Vthlim, TBLK, Iscp, Vthscp

Simulation Condition

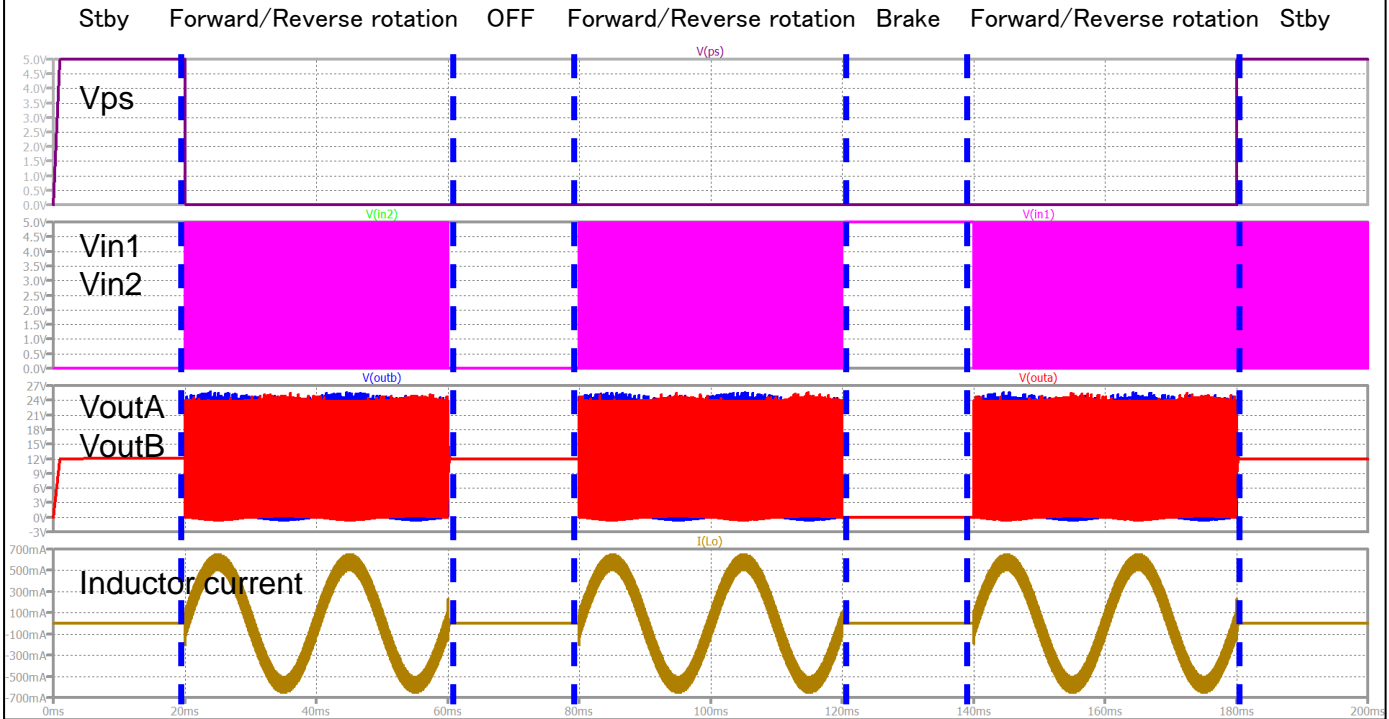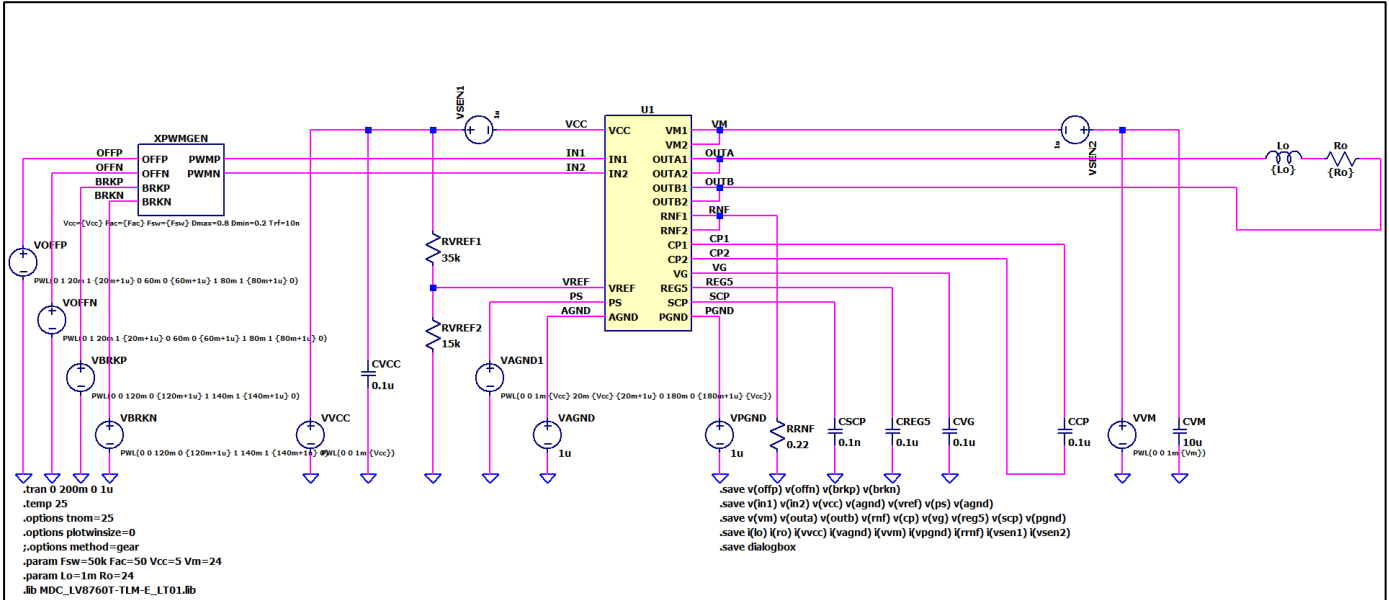This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition			Unit
	Min	Typ	Max	
Vm supply voltage	9		35	V
Vcc supply voltage	3		5.5	V
Temperature		25		deg C

Model Functions Table

Functions	Implemented
DCM output control logic	○
Current limit control	○
Output short-circuit protection function	○
UVLO	○

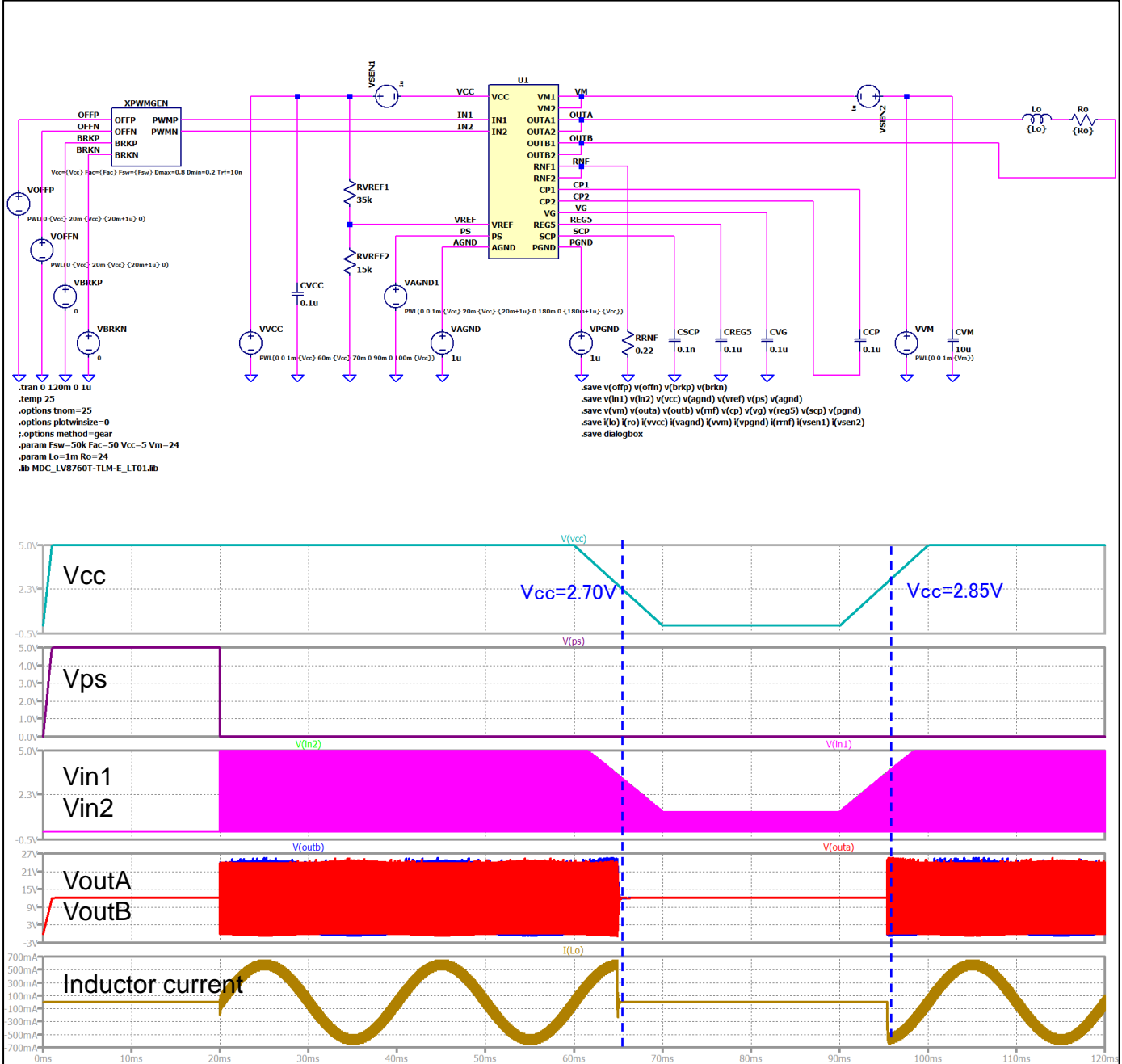**Testbench for PWM , brake, stand-by mode (PWM : Fin=50[Hz] Fc=50[kHz], Lo = 1[mH], Ro = 1[A])**

Referred to Data Sheet

Testbench for UVLO (Lout=1[nH] Rout=24[ohm])

Referred to Data Sheet

Testbench for OCP (PWM : Fin = 50[Hz] Fc= 50[kHz], Lo = 1[mH], Ro = 6[ohm], Vref = 1.5[V])

Referred to Data Sheet

DISCLAIMER

MoDeCH

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