

# LTspice Model

## Forward/Reverse H-bridge Driver

### ON Semiconductor

### LV8760T-TLM-E

#### Model Information

<b>Model</b>	A macro model
<b>Call Name</b>	MDC_LV8760T-TLM-E_LT
<b>Pin Assign</b>	1:PGND 2,3:OUTB 4,5:RNF 6,7:VM 8,9:OUTA 10:PS 11:GND 12:VG 13:CP2 14:CP1 15:REG5 16:IN1 17:IN2 18:VREF 19:SCP VCC
<b>File List</b>	Model Library MDC_LV8760T-TLM-E_LT02.lib Model Report MDC_LV8760T-TLM-E_LT.pdf(this file)
<b>Verified Simulator Version</b>	LTspice XVII

#### Note

#### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version August, 2013
- Product name LV8760T-TLM-E
- Company name ON Semiconductor

[Characteristics listed]

- Characteristics VREG, VthVCC, VthHIS  
Ron1, Ron2, I0leak, tr, tf, tpLH, tpHL,  
VGH, tONG, Fcp, IINL, IINH, VINH, VINH,  
IREF, Vthlim, TBLK, Iscp, Vthscp

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

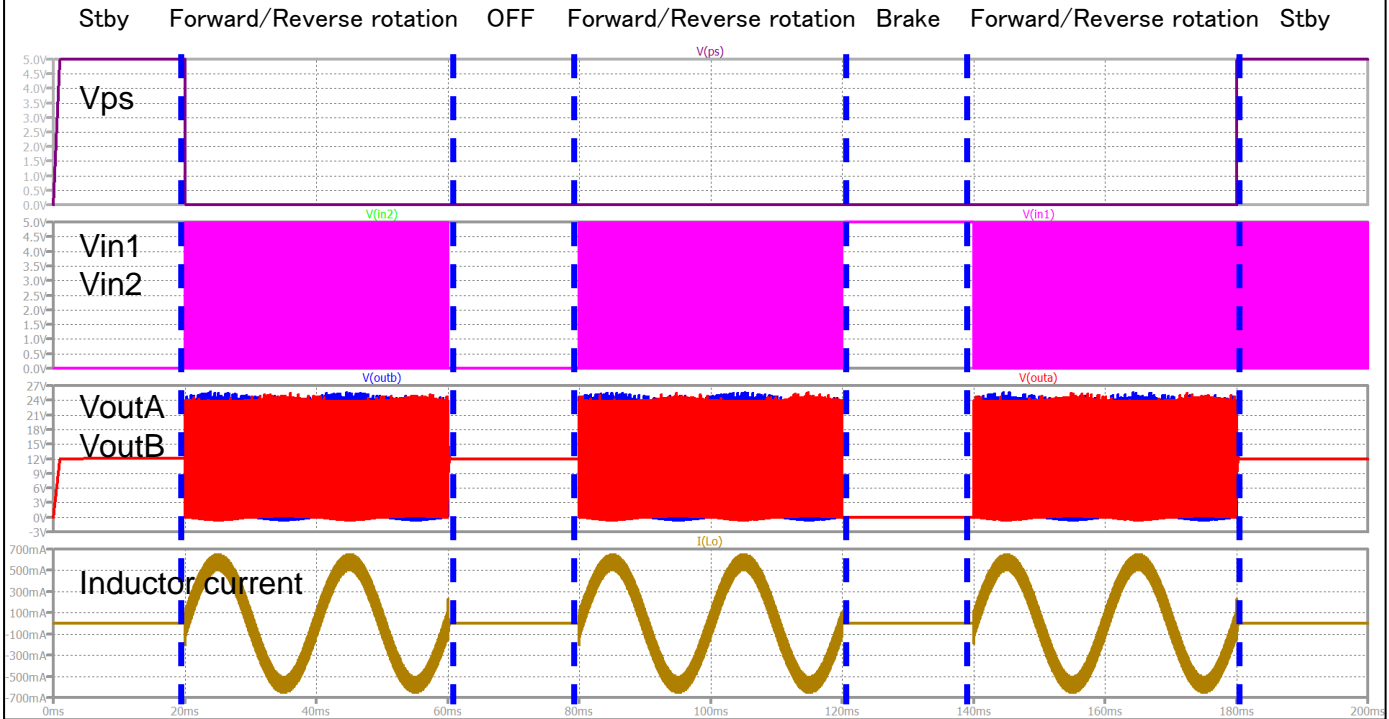
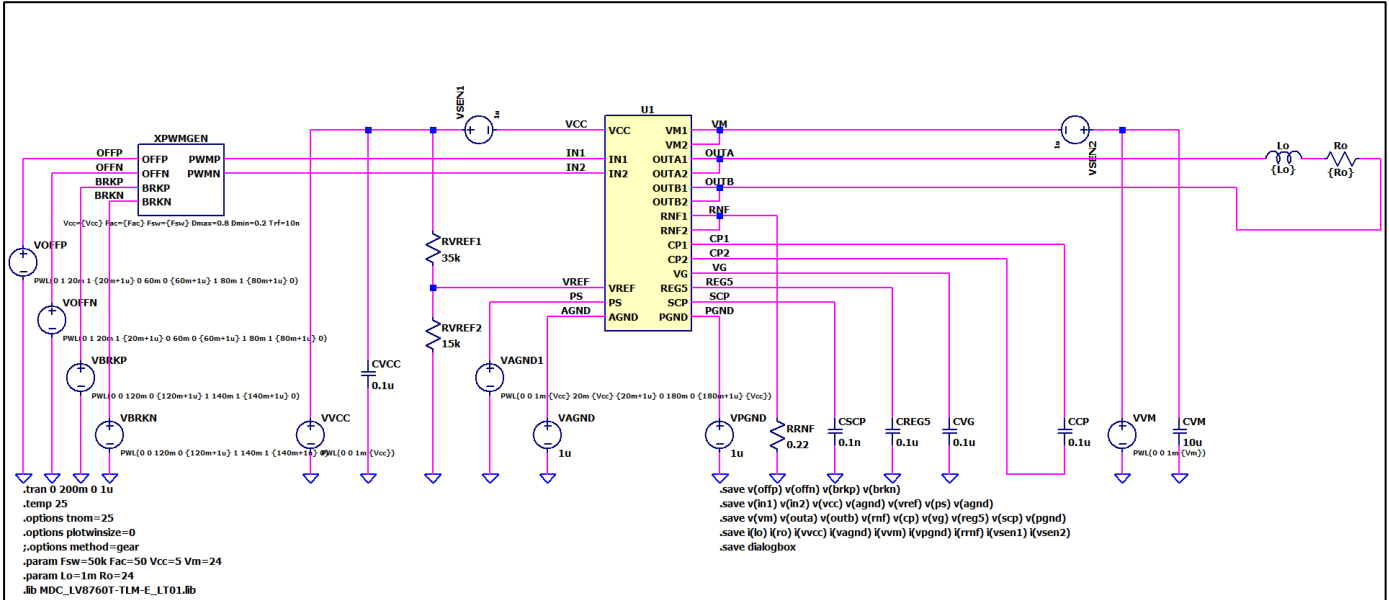
Item	Condition			Unit
	Min	Typ	Max	
Vm supply voltage	9		35	V
Vcc supply voltage	3		5.5	V
Temperature		25		deg C

**Model Functions Table**

Functions	Implemented
DCM output control logic	<input type="radio"/>
Current limit control	<input type="radio"/>
Output short-circuit protection function	<input type="radio"/>
UVLO	<input type="radio"/>

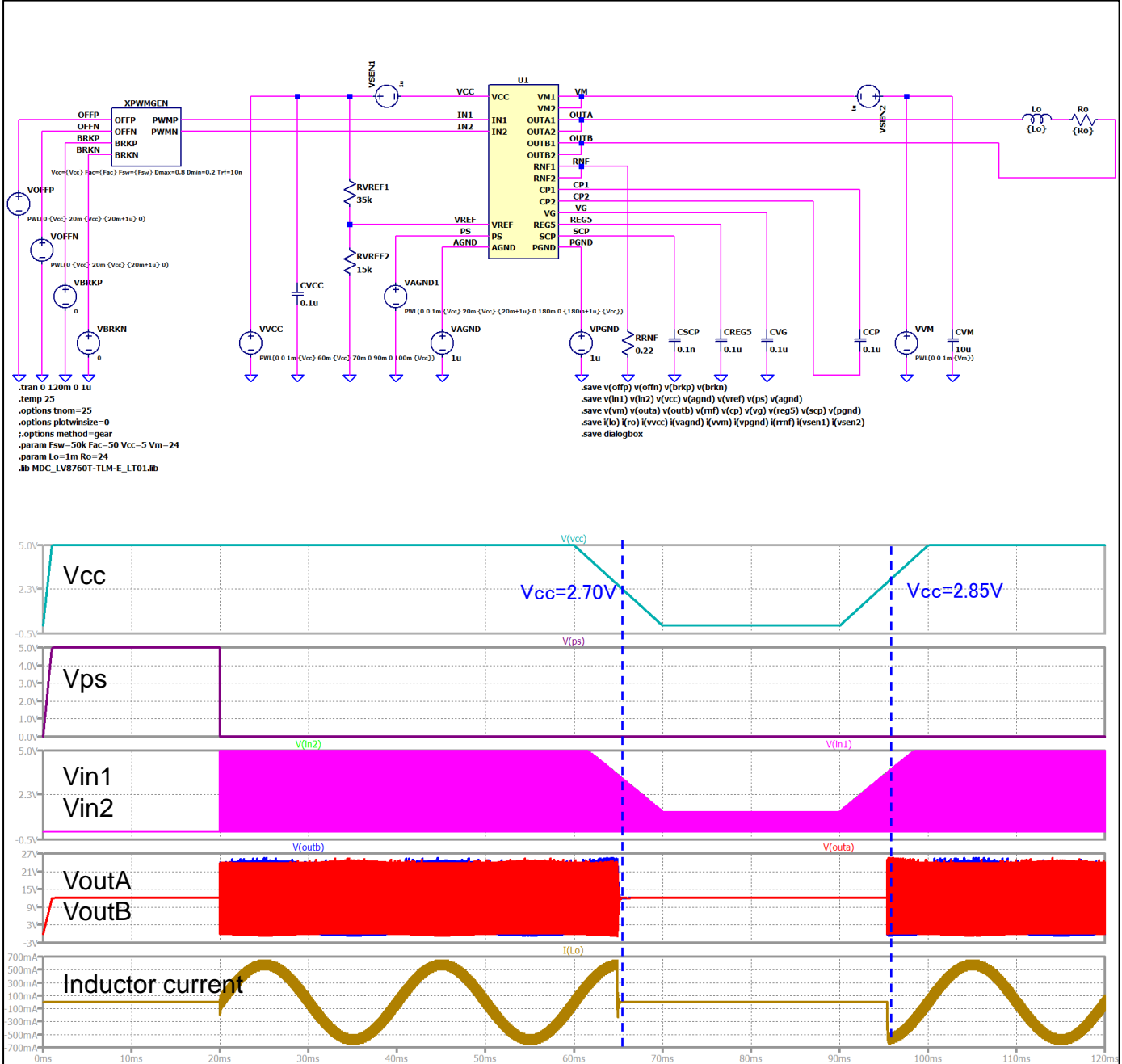
Testbench for PWM , brake, stand-by mode (PWM :  $F_{in}=50[Hz]$   $F_c=50[kHz]$ ,  $L_o = 1[mH]$ ,  $R_o = 1[A]$ )

Referred to Data Sheet



Testbench for UVLO (Lout=1[nH] Rout=24[ohm])

Referred to Data Sheet





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