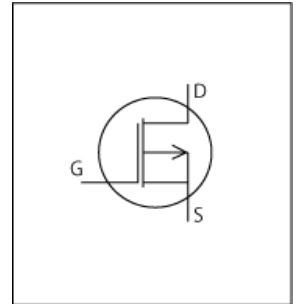


LTspice Model

PMOS

AOS

AOD4185



Model Information

Model A macro model based on BSIM3 model
Call Name MDC_AOD4185_LT
Pin Assign 1:G 2:D 3:S
File List Model Library MDC_AOD4185_LT01.lib
 Model Report MDC_AOD4185_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Unknown
- Product name AOD4185
- Company name Alpha and Omega Semiconductor
- Characteristics IdVds[Vgs], IdVgs[Temp], Rds(on)Id[Vgs], Rds(on)Temp[Vgs], Rds(on)Temp[Vgs]02, Rds(on)Vgs[Temp], IsVsd[Temp], VgsQg[Vdd], CapacitanceVds[Cname], SwitchingIdd[Tname], TrrIf[Ir], QrrIf[Ir], YfsId[Temp], SwitchingWaveform, TrrQrrWaveform

Simulation Range

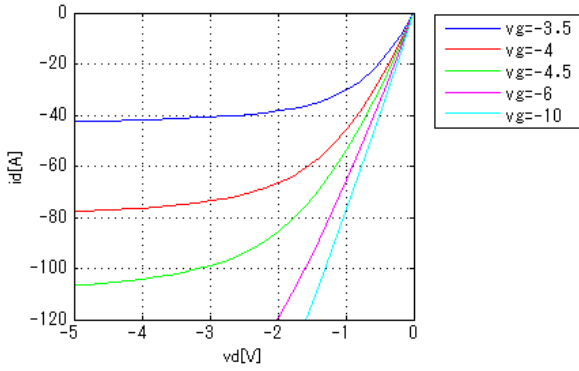
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	-40	V
Gate-source voltage (DC)	20	to	-20	V
Temperature	-55	to	175	deg C

Simulation results are following.
 Explanatory notes — : simulated

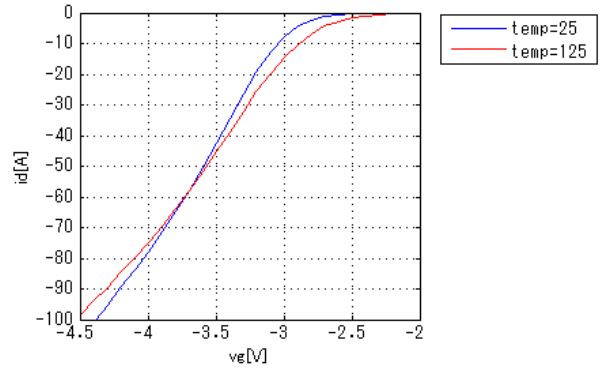
IdVds[Vgs]

Temp. = 25degC

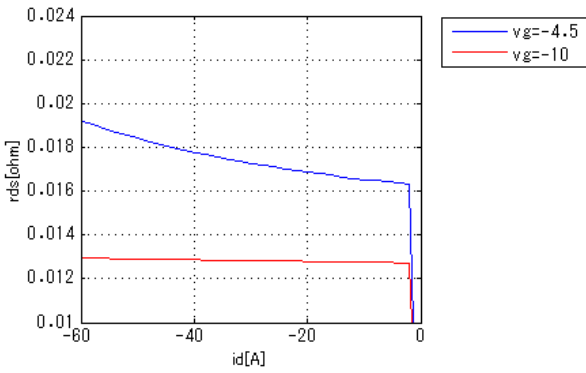


IdVgs[Temp]

$V_{ds} = -5V$

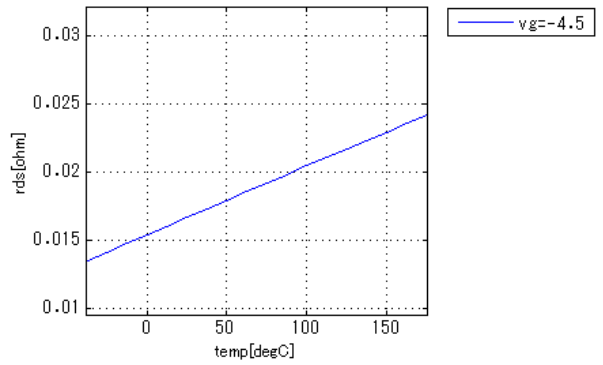


Rds(on)Id[Vgs]



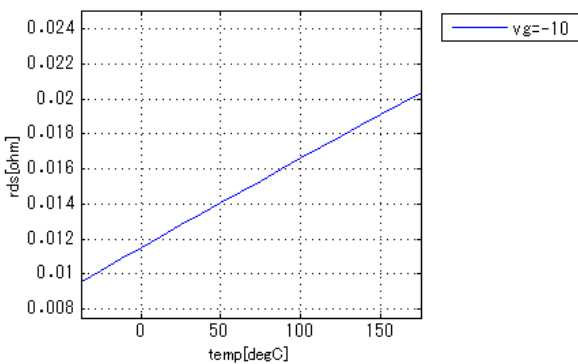
Rds(on)Temp[Vgs]

$I_d = -15A$



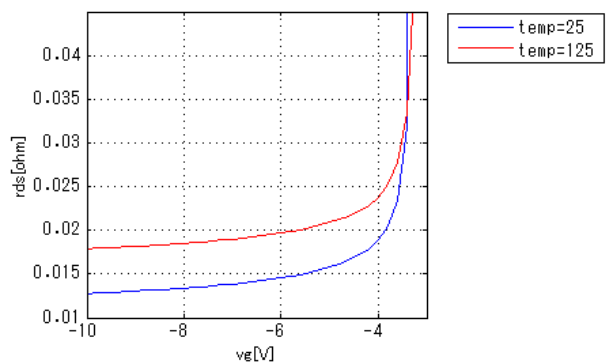
Rds(on)Temp[Vgs]02

$I_d = -20A$



Rds(on)Vgs[Temp]

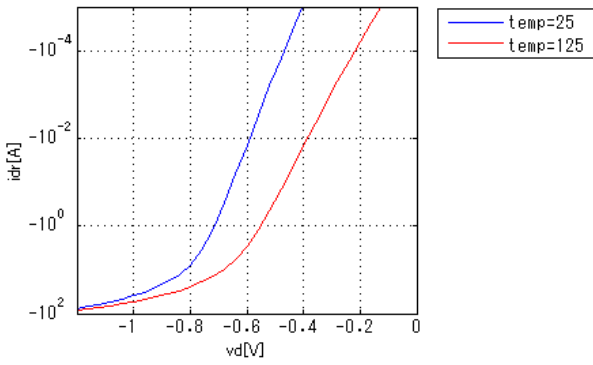
$I_d = -20A$



Simulation results are following.
 Explanatory notes — : simulated

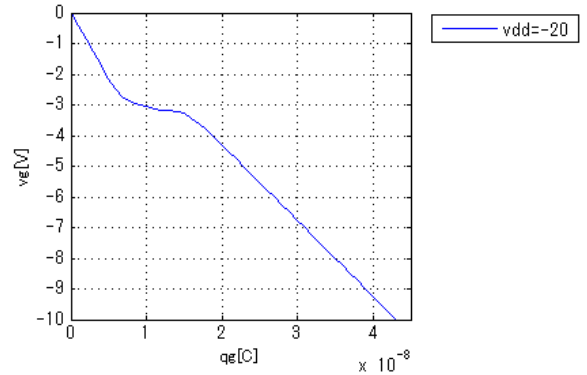
IsVsd[Temp]

vg = 0V



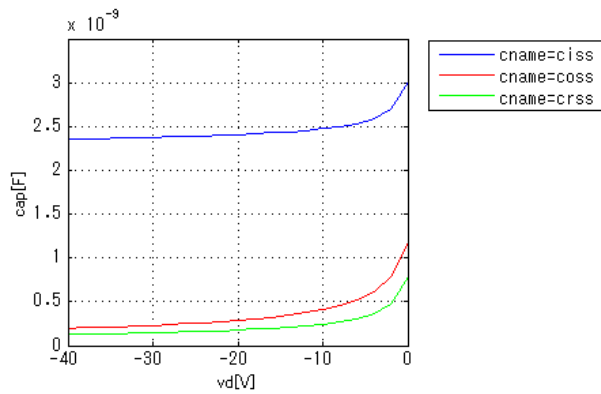
VgsQg[Vdd]

Id = A



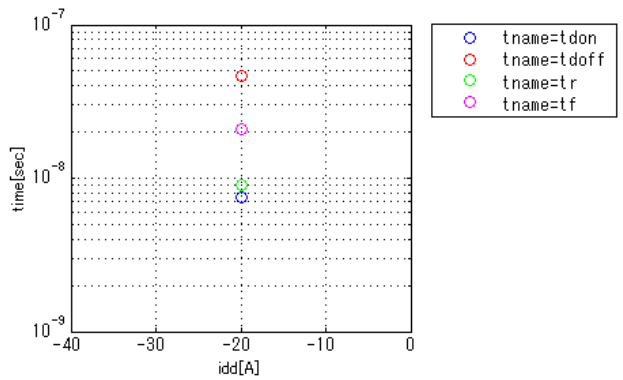
CapacitanceVds[Cname]

freq = 1000000Hz



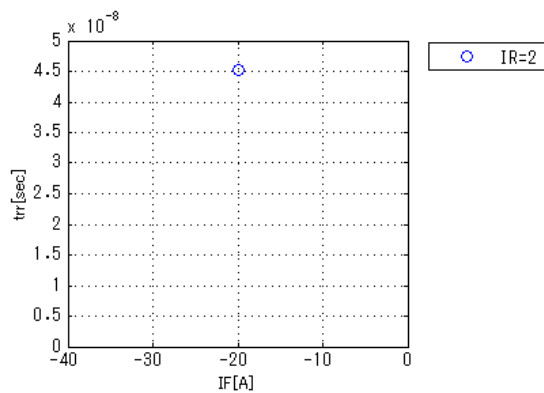
SwitchingIdd[Tname]

vgg = -10V, vdd = -20V, RGG = 3ohm



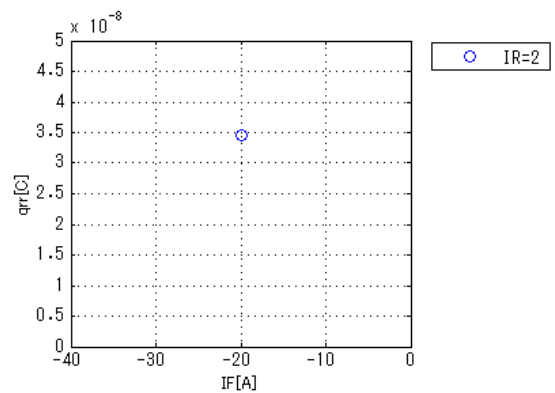
Trrlf[Ir]

vdd = 0V, didt = 100A/us



Qrrlf[Ir]

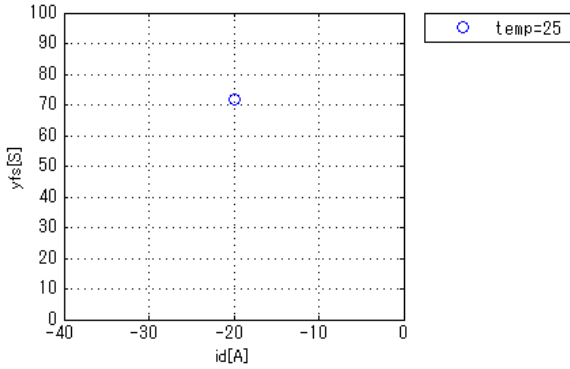
vdd = 0V, didt = 100A/us



Simulation results are following.
 Explanatory notes — : simulated

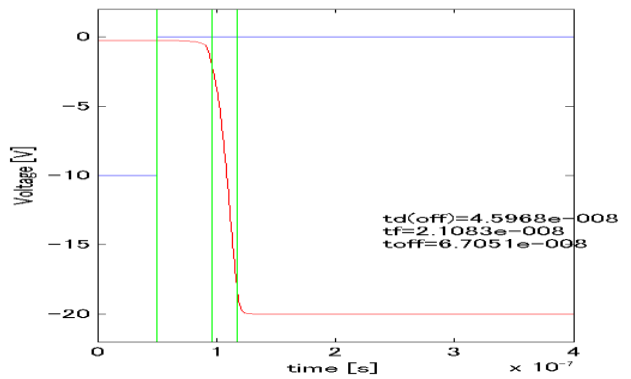
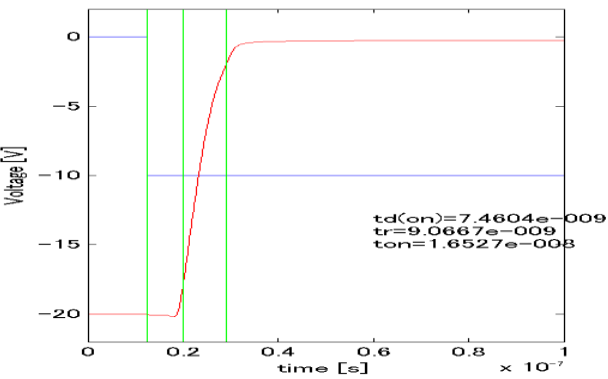
YfsId[Temp]

Vds = -5V



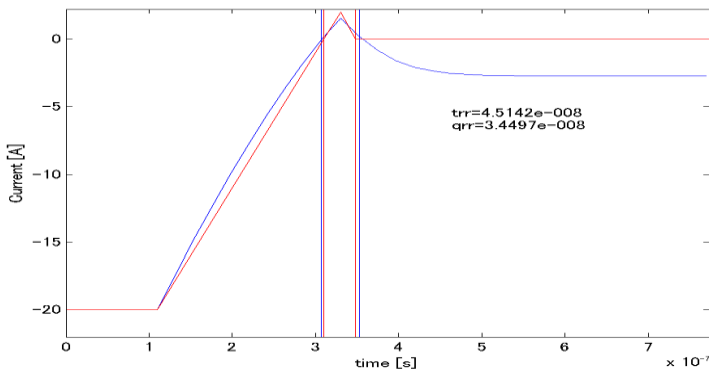
Switching Waveform

Blue : INPUT Red : OUTPUT



Trr Qrr Waveform

Red : Datasheet Blue : Simulation



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