

LTspice Model

Operational Amplifier

Nisshinbo Micro Devices Inc.

NJM2904CG

Model Information

Model A macro model
Call Name MDC_NJM2904CG_LT
Pin Assign 1:AOUTPUT 2:A-INPUT 3:A+INPUT 4:V- 5:B+INPUT 6:B-INPUT 7:BOOUTPUT 8:V+
File List Model Library MDC_NJM2904CG_LT.lib
 Model Report MDC_NJM2904CG_LT.pdf(this file)

Verified Simulator Version LTspice(x64) 17.1.15

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2023.10.13 Ver.14
- Product name NJM2904C/NJM2904CA
- Company name Nisshinbo Micro Devices Inc.(NreJRC)

[Characteristics listed]

- Characteristics Open Loop Gain
- Input offset voltage
- Input offset current
- Input bias current
- Output current limit
- Slew Rate

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

○ : Implemented
 × : Not Implemented
 — : Not applicable

Model Functions Table
RANK=1

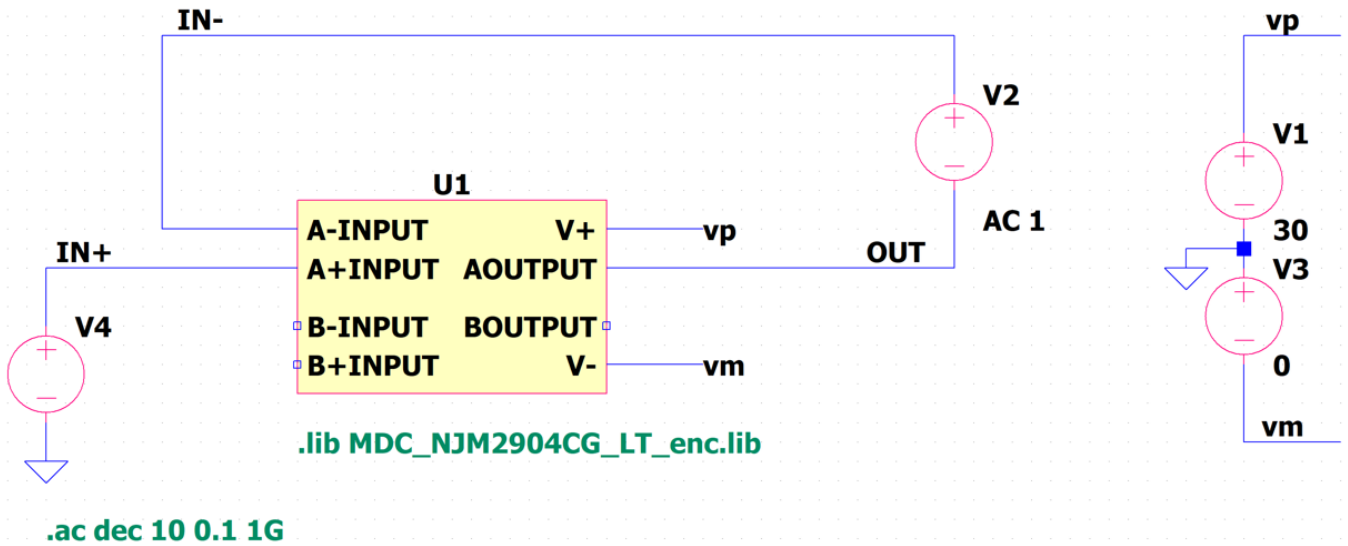
Functions	RANK	Implemented
Open Loop Gain	1	○
Unity Frequency	1	○
Phase Margin	1	—
Input Offset Voltage	1	○
Input Offset Current	1	○
Bias Current	1	○
Maximum output amplitude voltage	1	○
Slew Rate	1	○
Equivalent Input Noise Voltage	2	—
Equivalent Input Noise Current	2	—

Open Loop Gain

Simulation results are following.

Explanatory notes — : simulated

Testbench

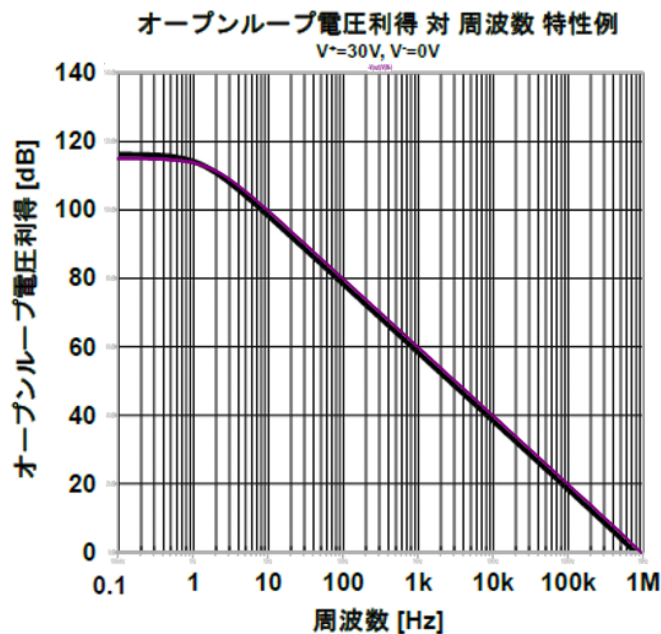


Open Loop Gain

Simulation results are following.

Explanatory notes — : simulated

Sim result

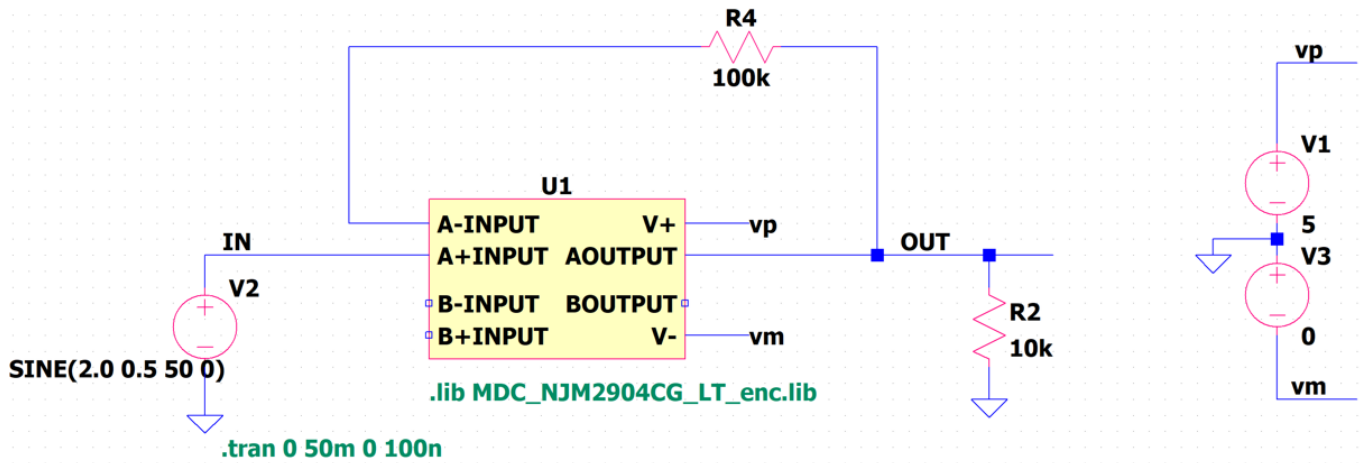


Input offset voltage

Simulation results are following.

Explanatory notes — : simulated

Testbench

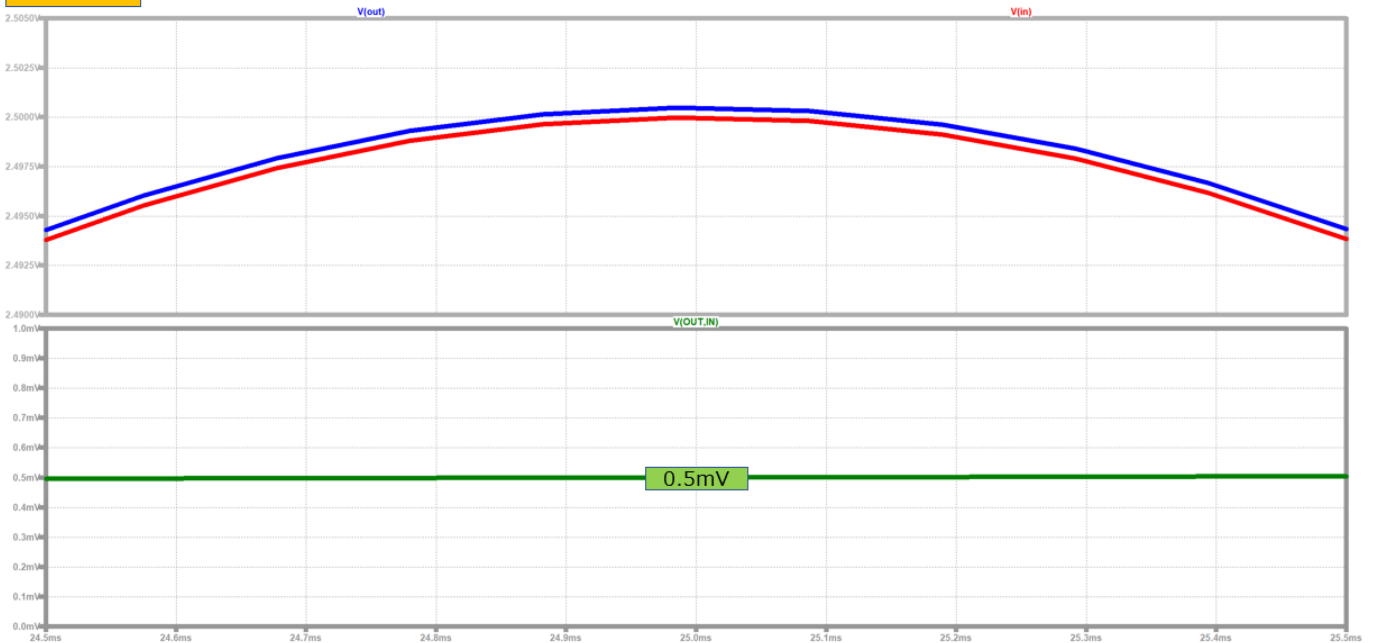


Input offset voltage

Simulation results are following.

Explanatory notes — : simulated

Sim result

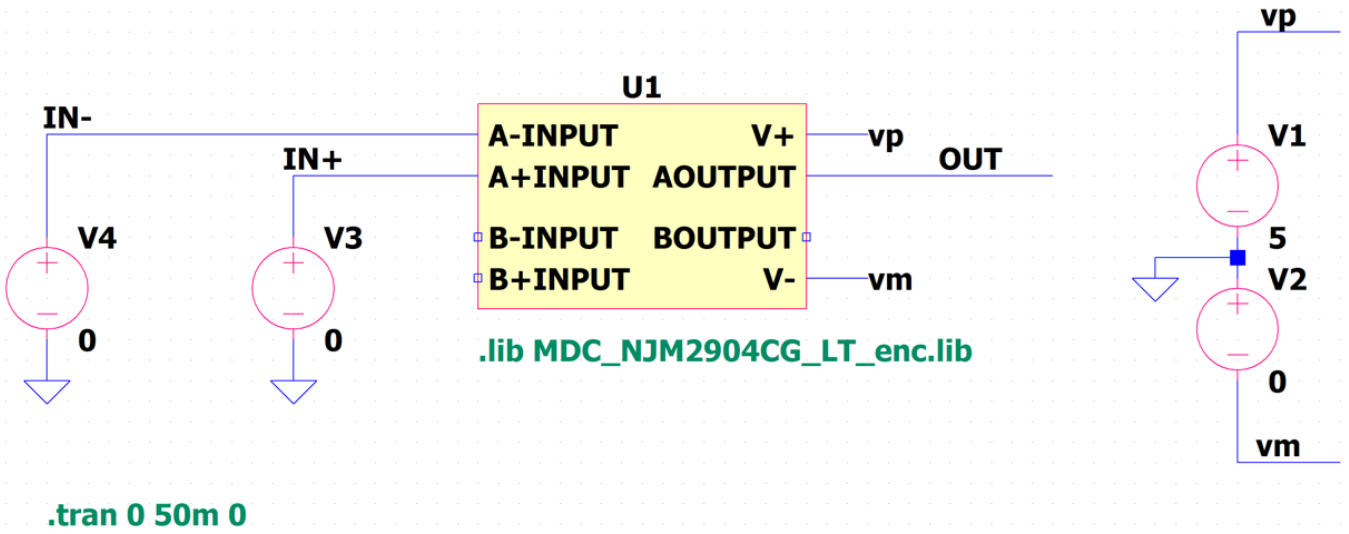


Input offset current

Simulation results are following.

Explanatory notes — : simulated

Testbench



Input offset current

Simulation results are following.

Explanatory notes — : simulated

Sim result

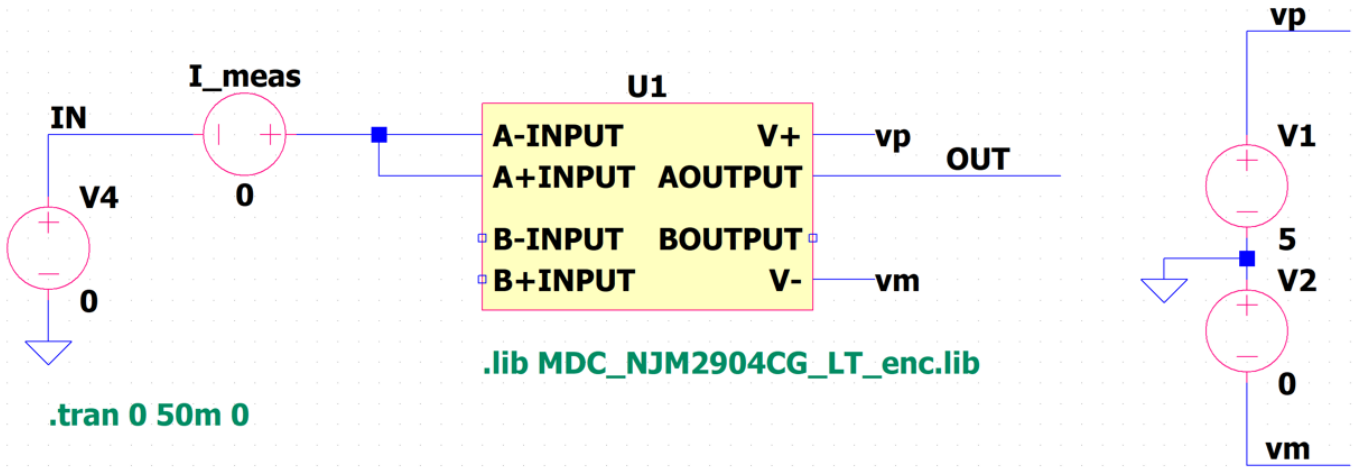


Input bias current

Simulation results are following.

Explanatory notes — : simulated

Testbench

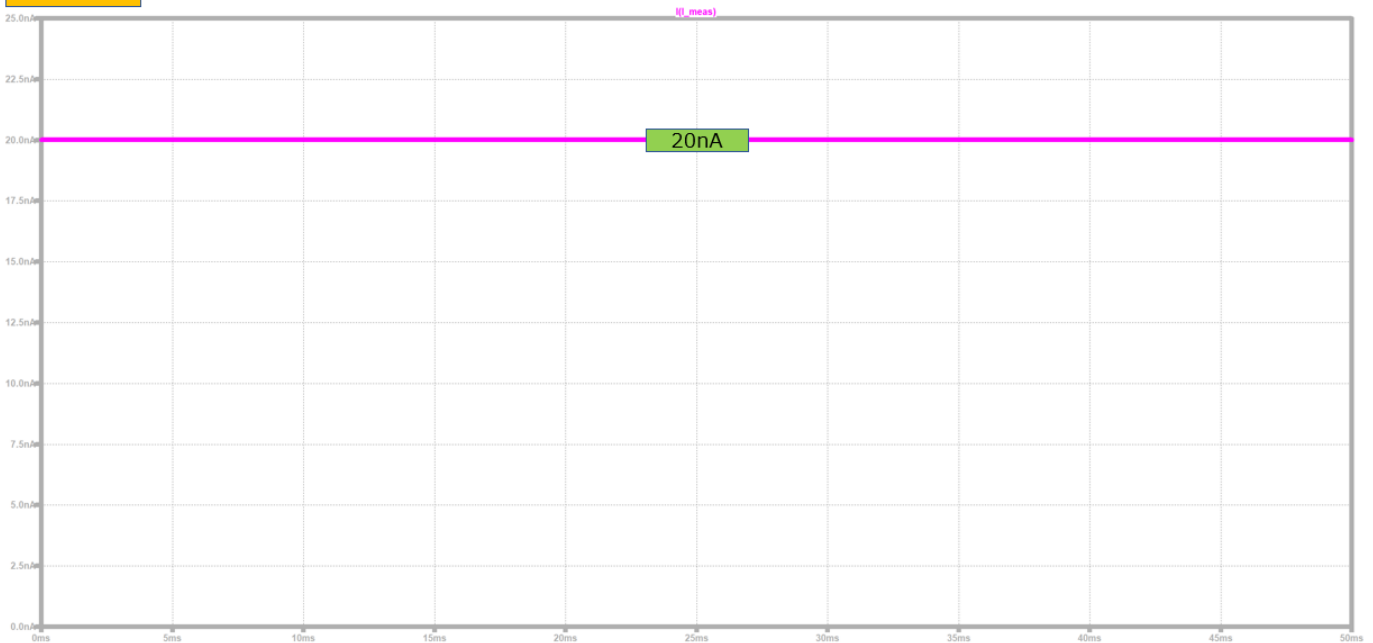


Input bias current

Simulation results are following.

Explanatory notes — : simulated

Sim result

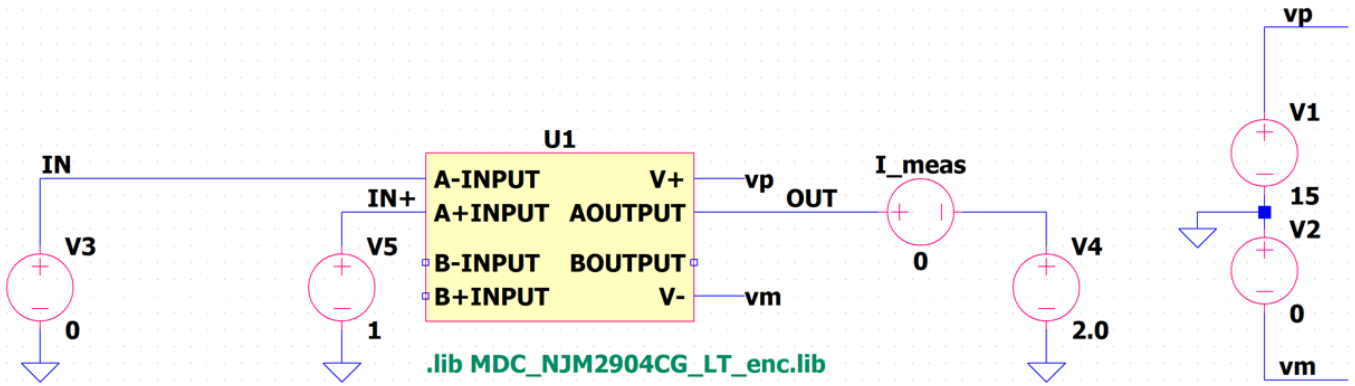


Output current limit(Source Current)

Simulation results are following.

Explanatory notes — : simulated

Testbench



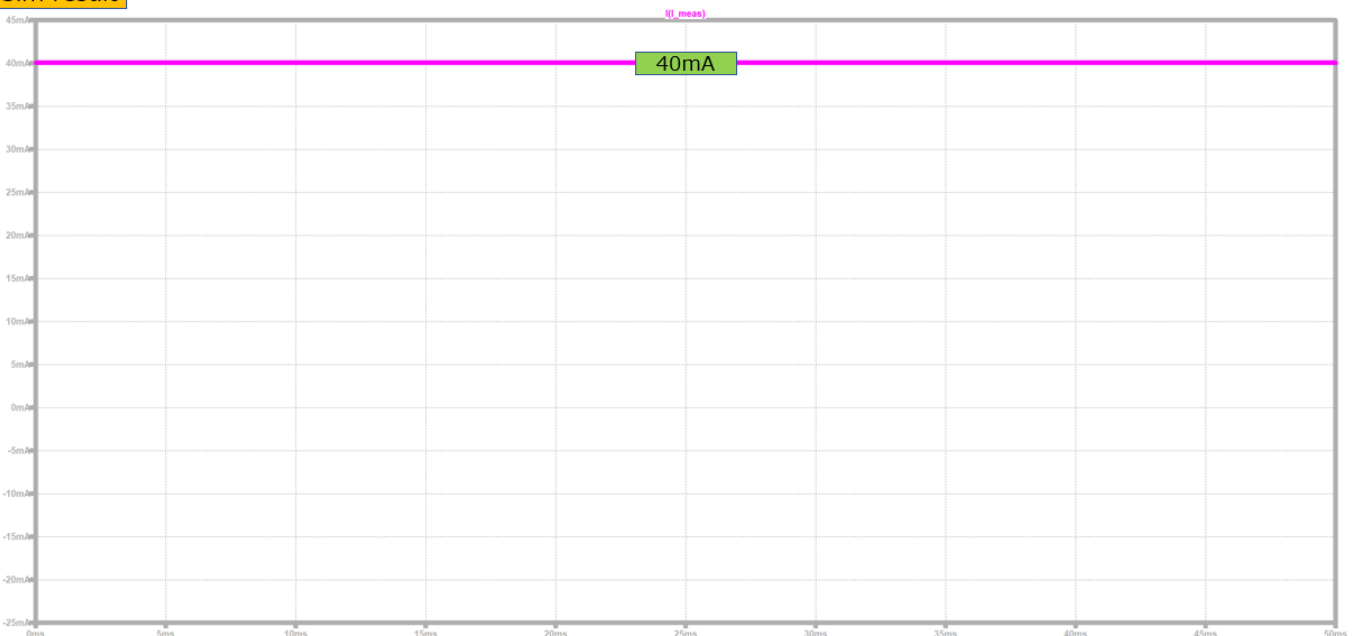
.tran 0 50m 0

Output current limit(Source Current)

Simulation results are following.

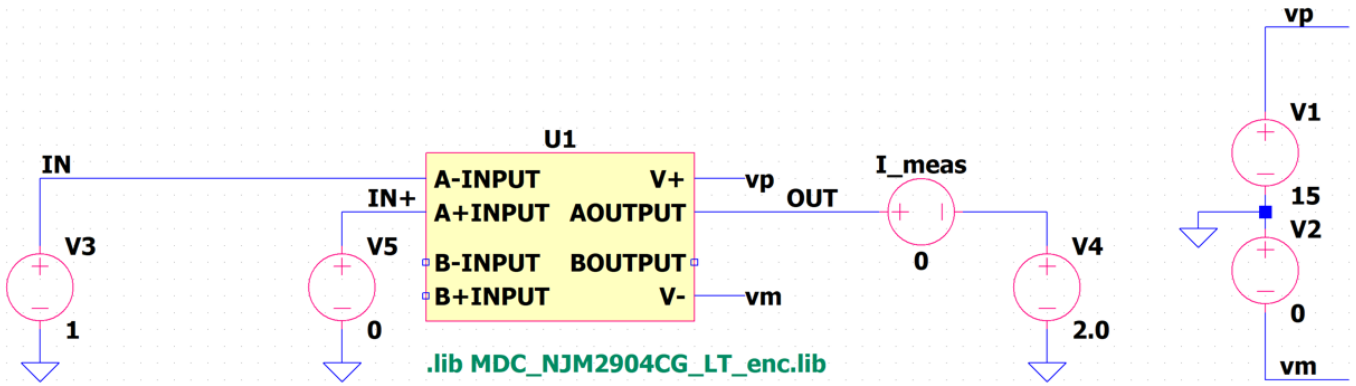
Explanatory notes — : simulated

Sim result



Output current limit(Sink Current)
 Simulation results are following.
 Explanatory notes — : simulated

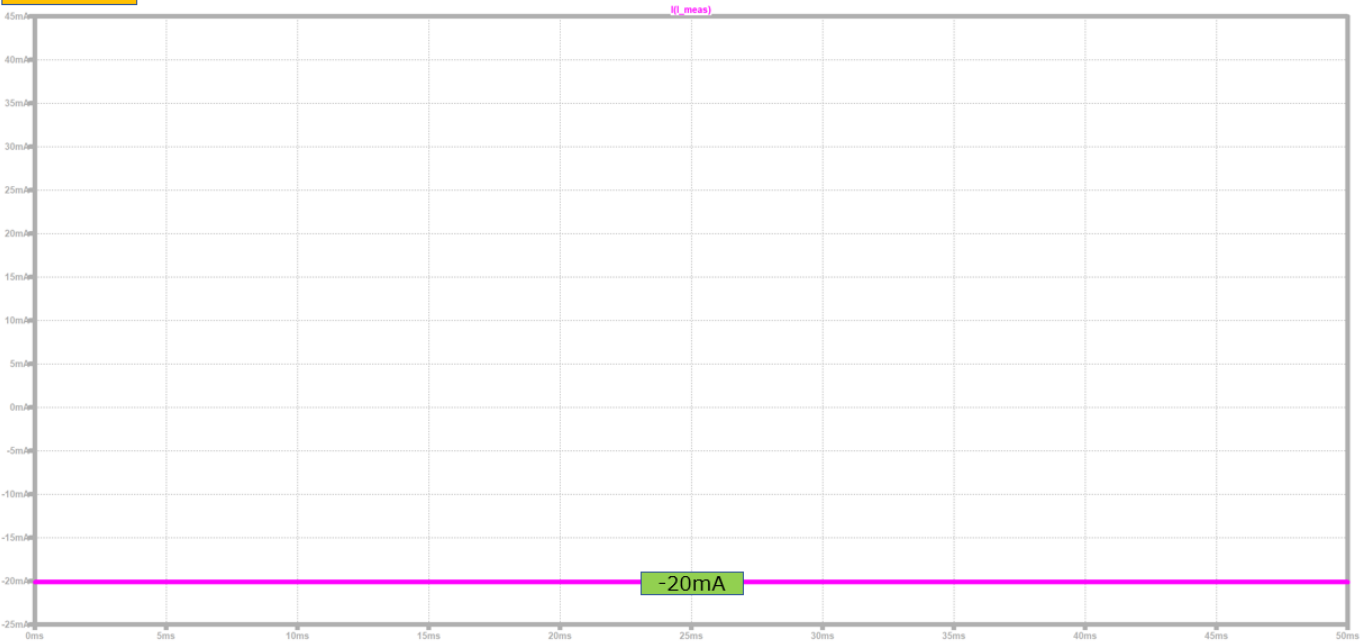
Testbench



`.tran 0 50m 0`

Output current limit(Sink Current)
 Simulation results are following.
 Explanatory notes — : simulated

Sim result

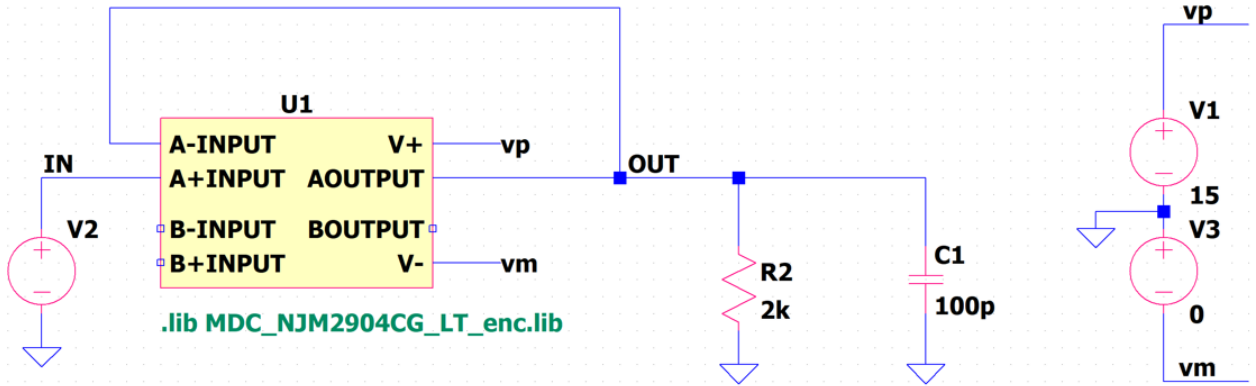


Slew Rate

Simulation results are following.

Explanatory notes — : simulated

Testbench



PULSE(0 1 2u 1n 1n 1u 6u)

.tran 0 40u 0 100n

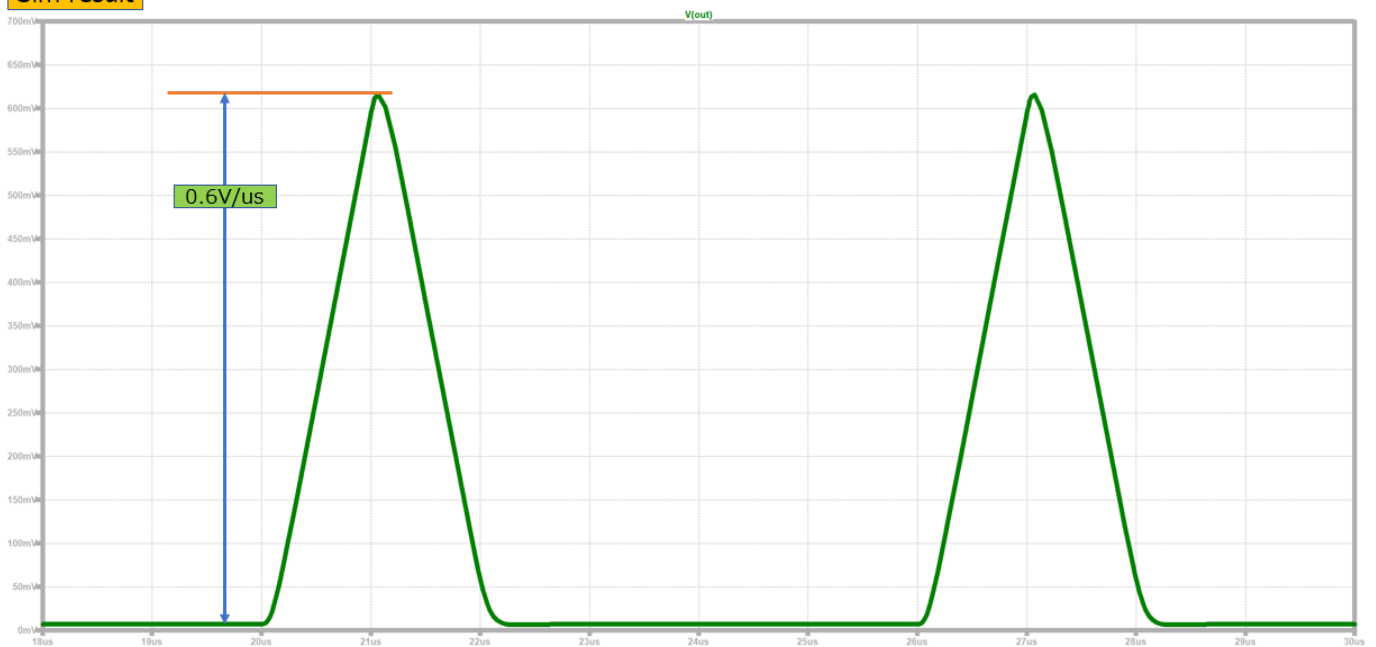
.meas VO_PP PP V(OUT) FROM 18u TO 30u

Slew Rate

Simulation results are following.

Explanatory notes — : simulated

Sim result



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