

LTspice Model

High voltage high and low-side driver

STMicroelectronics

L6391DTR

Model Information

Model A macro model
Call Name MDC_L6391DTR_LT
Pin Assign 1:_LIN 2:_SD/OD 3:HIN 4:VCC 5:DT 6:NC1 7:AGND 8:CP- 9:CP+ 10:LVG 11:NC2 12:OUT
 13:HVG 14:BOOT
File List Model Library MDC_L6391DTR_LT01.lib
 Model Report MDC_L6391DTR_LT.pdf (this file)
Verified Simulator Version LTspice XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version September 2015 DocID17892 Rev 3
- Product name L6391DTR
- Company name STMicroelectronics

[Characteristics listed]

- Characteristics Truth Table, UVLO
Switching, Dead Time

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

Driver

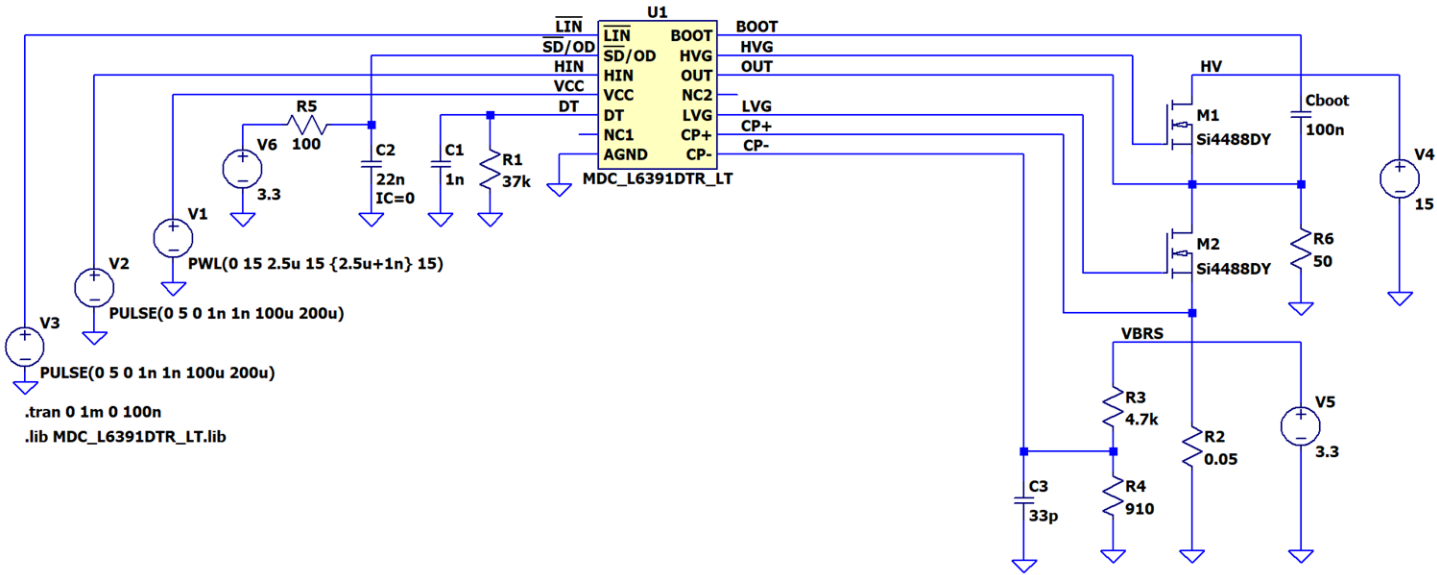
○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table
RANK=1

Functions	RANK	Implemented
Truth Table	1	○
On Resistance	1	○
Switching(Typ.)	1	○
UVLO	1	○
VH/VIL-VDD	1	—
Clamp Voltage	1	—
Propagation delay	1	○
Over Current Protection	2	—
Over Voltage Protection	2	—

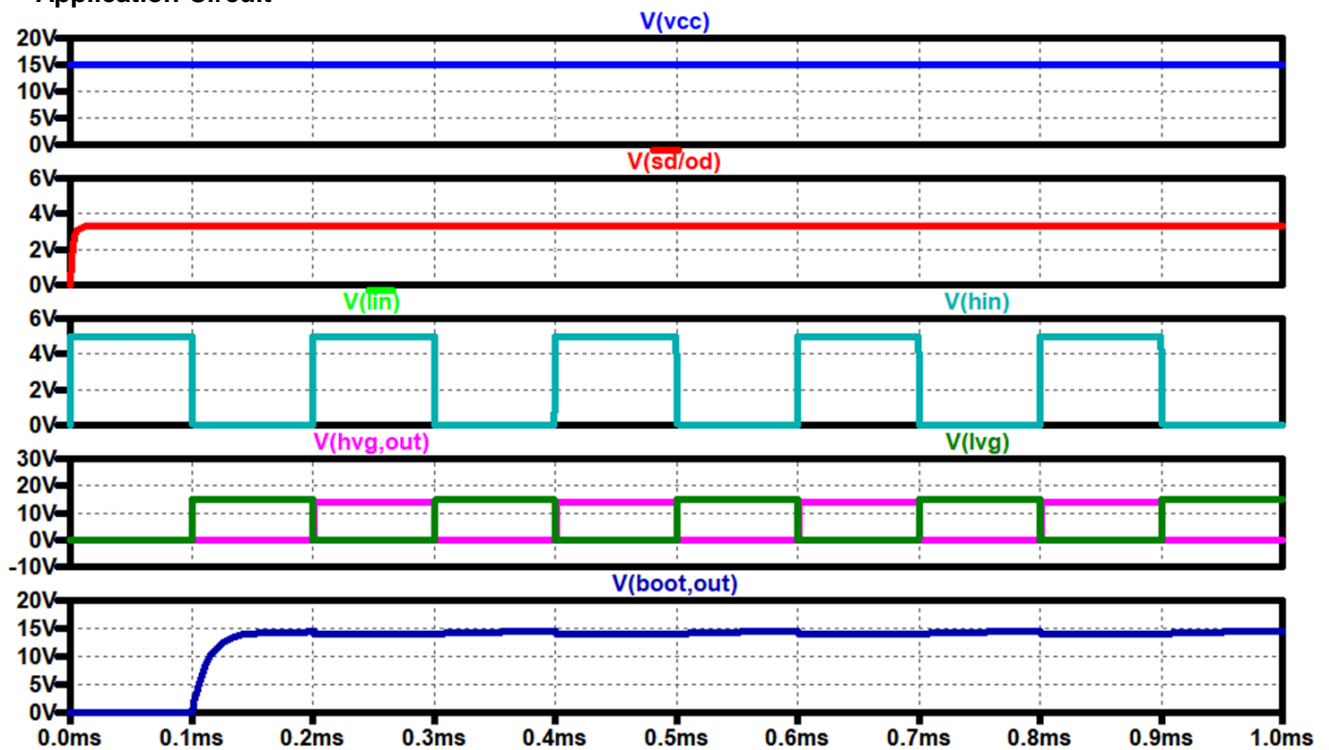
Application Circuit (Vcc = 15V, H.V. = 15V, TOLOAD = 50Ω) Testbench

Referred to Data Sheet



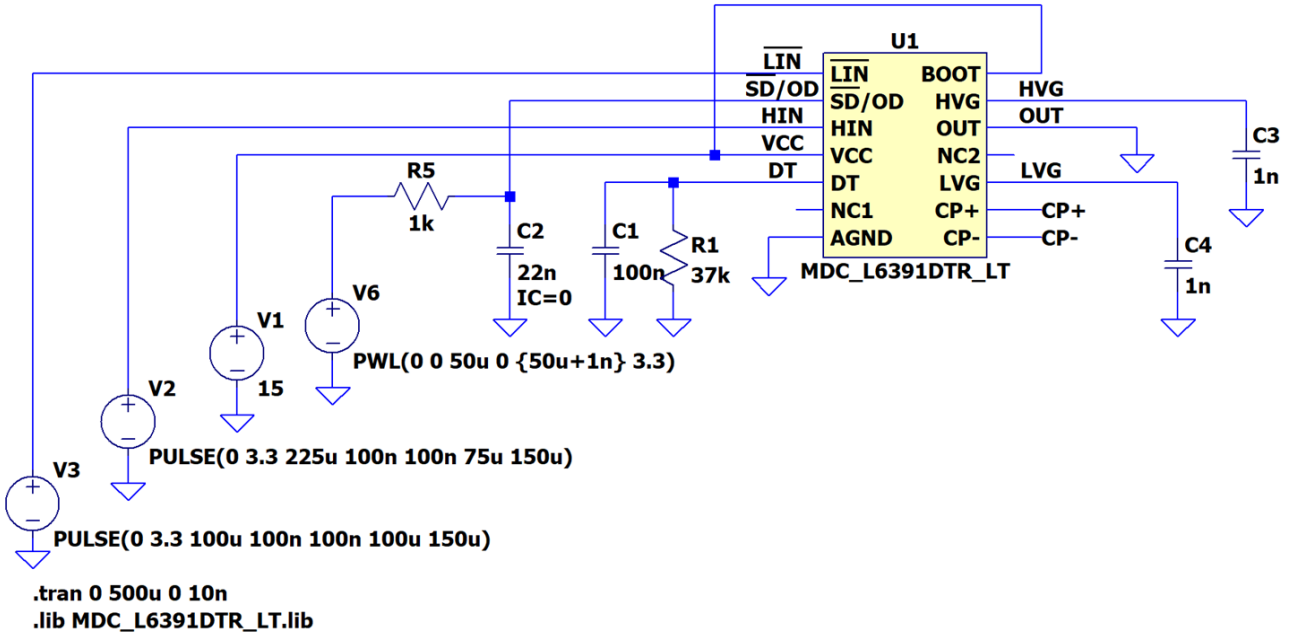
Simulation results are following.
 Explanatory notes — : simulated

Application Circuit



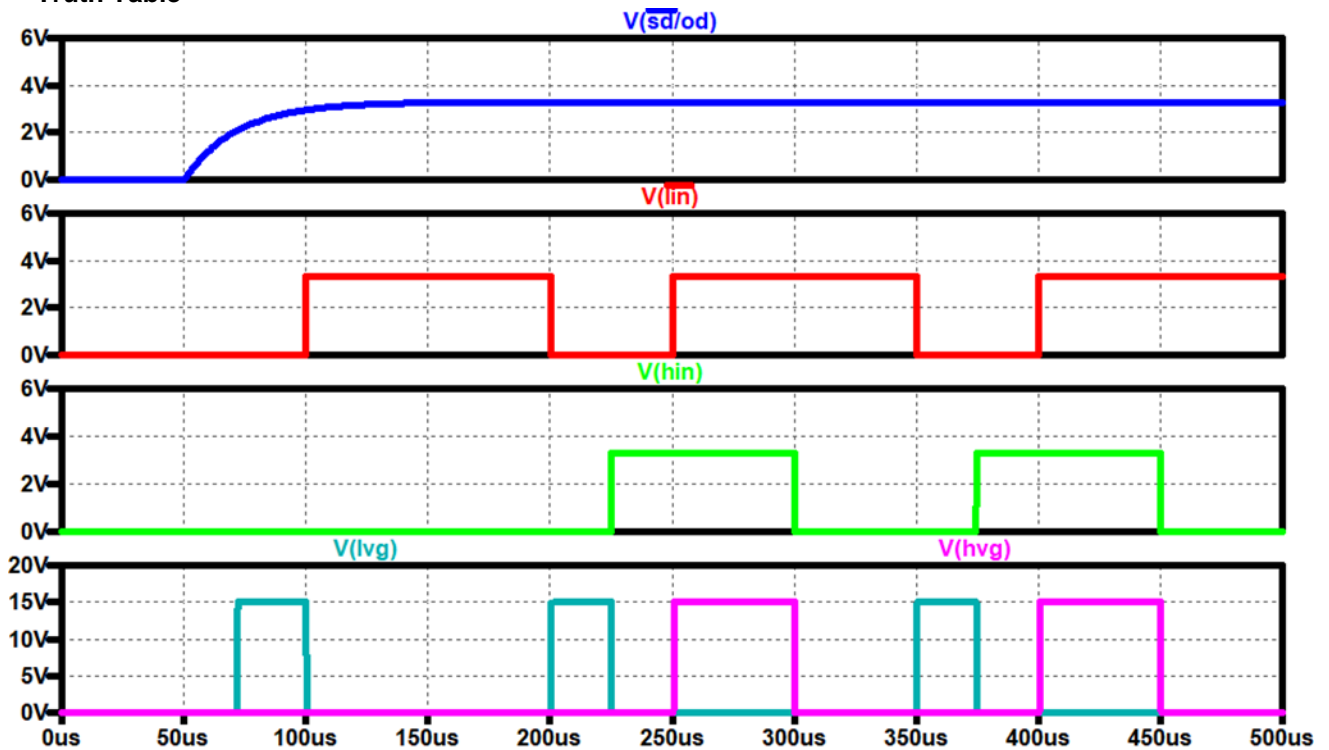
Truth Table Testbench

Referred to Data Sheet



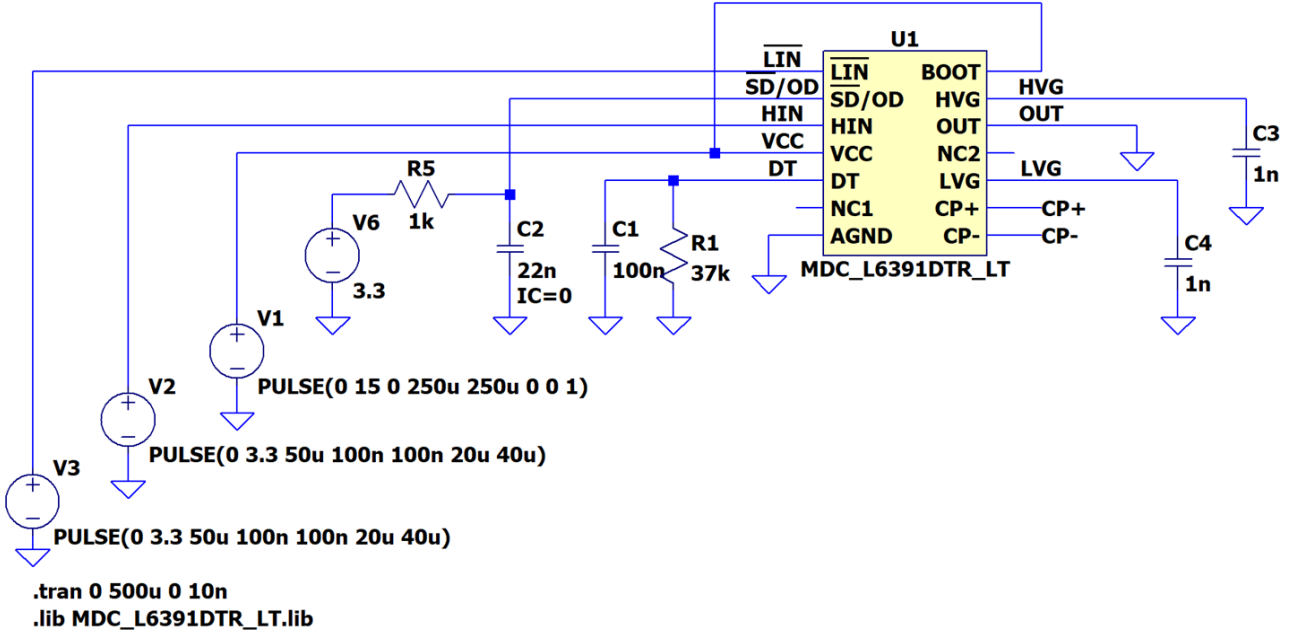
Simulation results are following.
Explanatory notes — : simulated

Truth Table



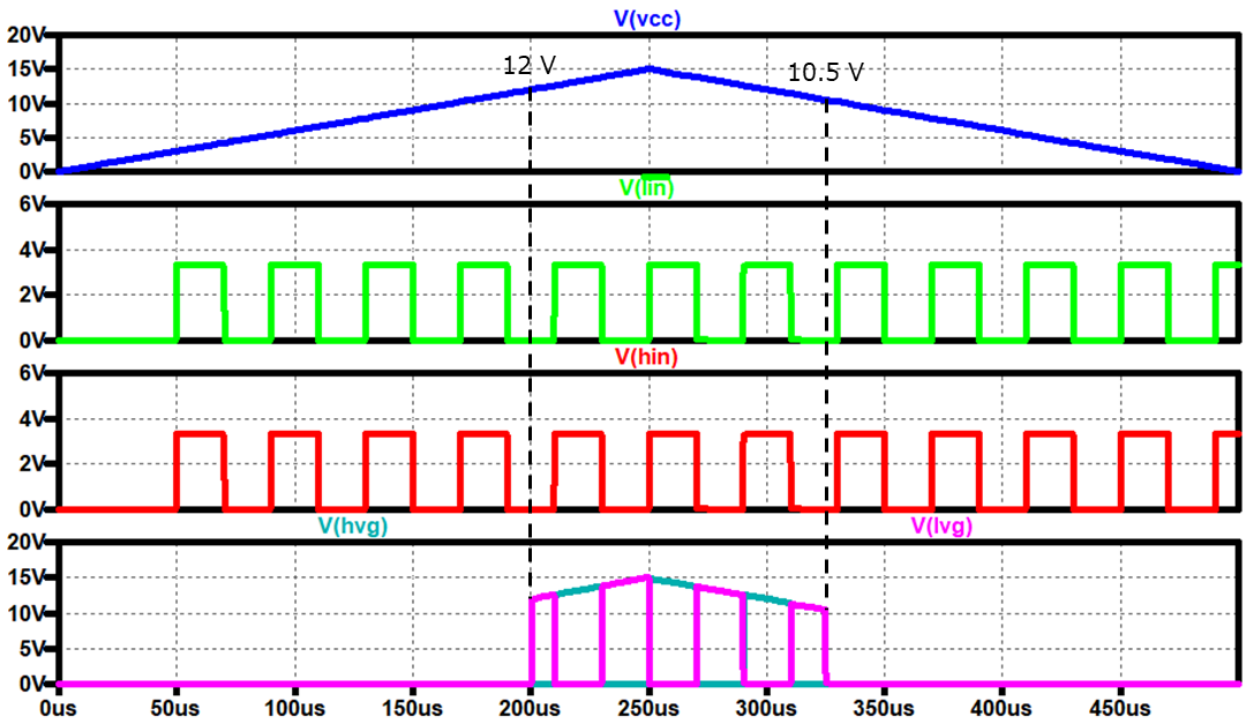
VccUVLO Testbench

Referred to Data Sheet



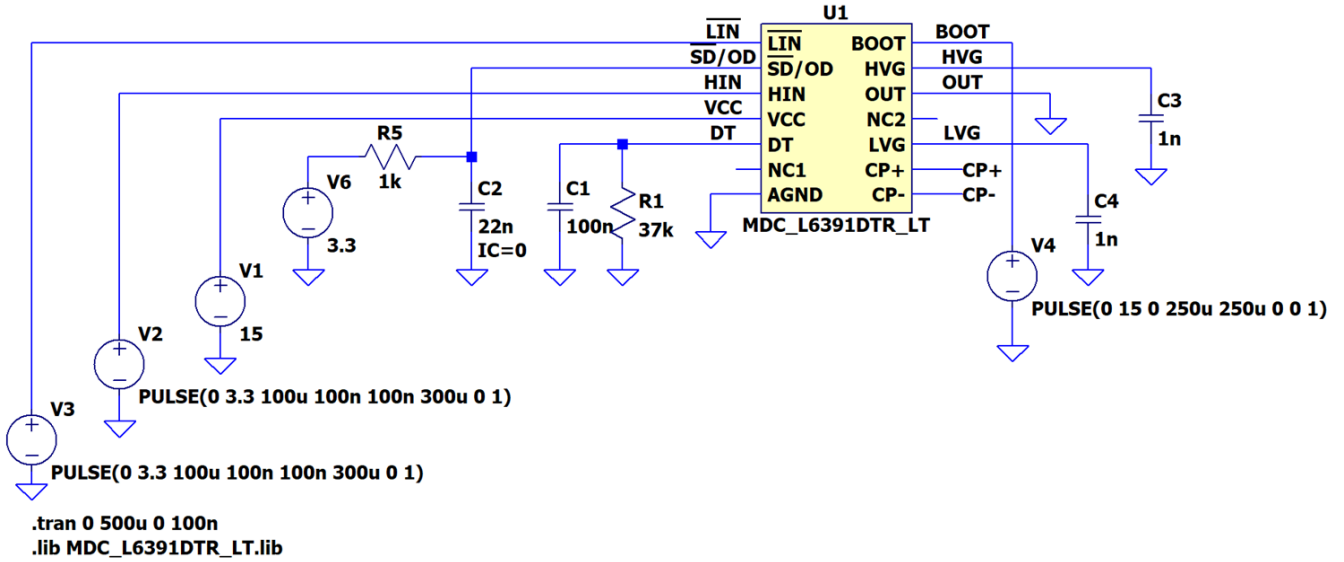
Simulation results are following.
 Explanatory notes — : simulated

VccUVLO



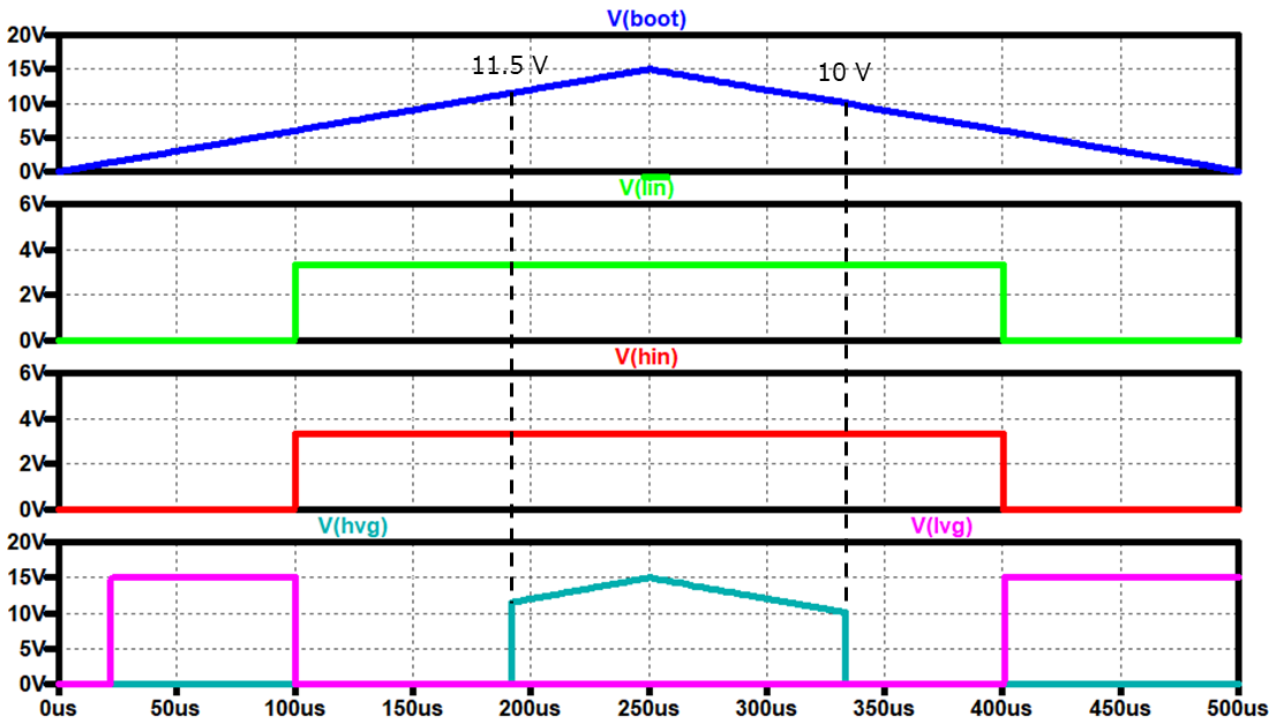
VboUVLO Testbench

Referred to Data Sheet



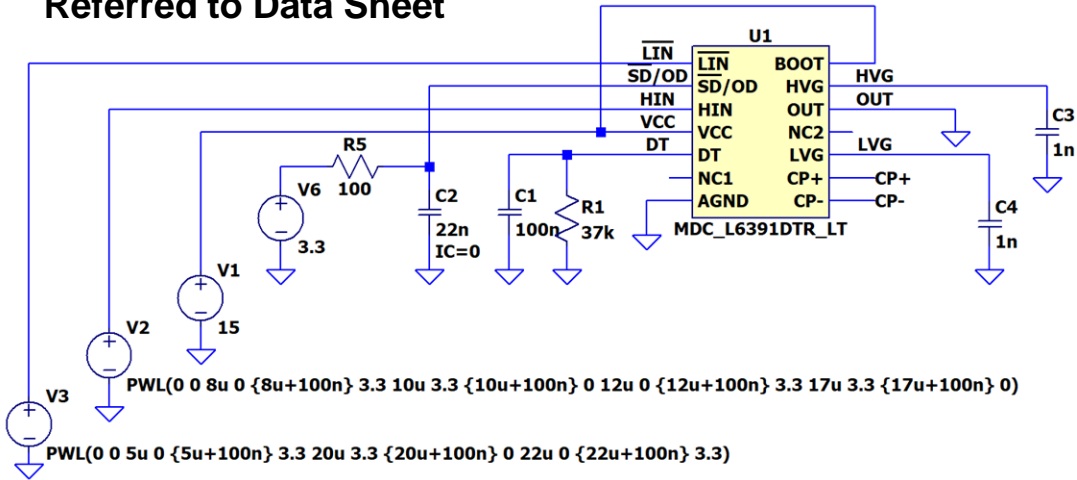
Simulation results are following.
 Explanatory notes — : simulated

VboUVLO



Switching Testbench

Referred to Data Sheet

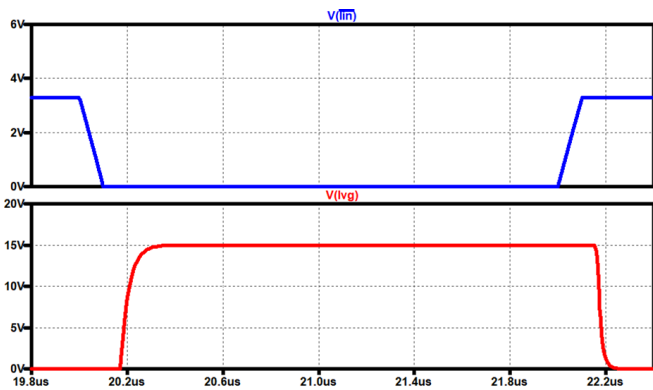


```
.tran 0 25u 0 10n
.lib MDC_L6391DTR_LT.lib
.meas TRAN Linr FIND V(LIN) WHEN V(LIN) = 3.3*0.5 CROSS=3
.meas TRAN Linf FIND V(LIN) WHEN V(LIN) = 3.3*0.5 CROSS=2
.meas TRAN Ltr10% FIND V(LVG) WHEN V(LVG) = 15*0.1 CROSS=3
.meas TRAN Ltr90% FIND V(LVG) WHEN V(LVG) = 15*0.9 CROSS=3
.meas TRAN Ltf10% FIND V(LVG) WHEN V(LVG) = 15*0.1 CROSS=4
.meas TRAN Ltf90% FIND V(LVG) WHEN V(LVG) = 15*0.9 CROSS=4
.meas TRAN Hintr FIND V(HIN) WHEN V(HIN) = 3.3*0.5 CROSS=1
.meas TRAN Hinf FIND V(HIN) WHEN V(HIN) = 3.3*0.5 CROSS=2
.meas TRAN Htr10% FIND V(HVG) WHEN V(HVG) = 15*0.1 CROSS=1
.meas TRAN Htr90% FIND V(HVG) WHEN V(HVG) = 15*0.9 CROSS=1
.meas TRAN Htf10% FIND V(HVG) WHEN V(HVG) = 15*0.1 CROSS=2
.meas TRAN Htf90% FIND V(HVG) WHEN V(HVG) = 15*0.9 CROSS=2
```

Simulation results are following.
Explanatory notes — : simulated

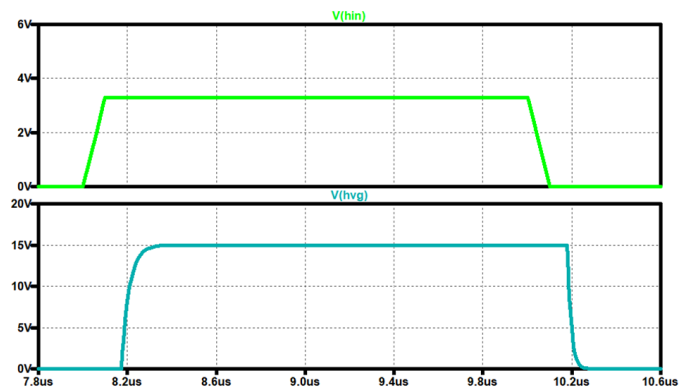
Switching

▪ Lside



t_{on}	125 ns
t_{off}	113 ns
t_r	75.1 ns
t_f	34.9 ns

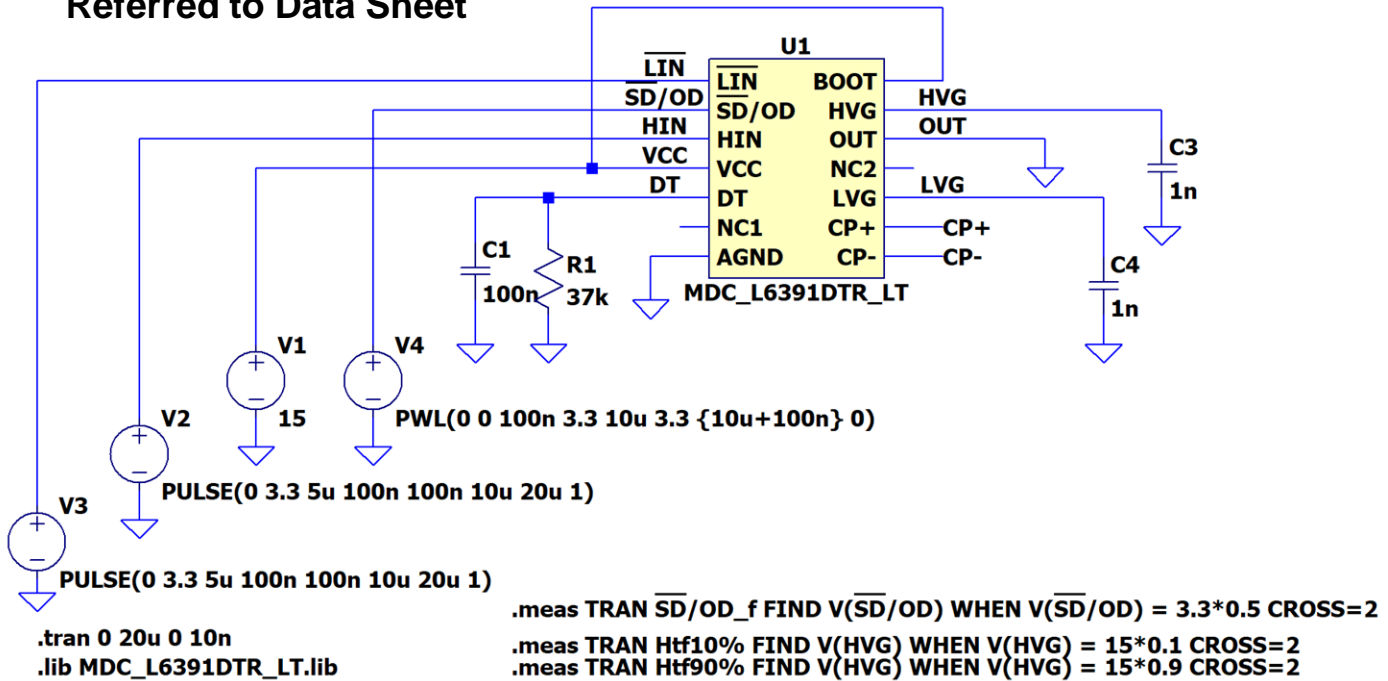
▪ Hside



t_{on}	126 ns
t_{off}	132 ns
t_r	75.1 ns
t_f	35.1 ns

Switching Testbench

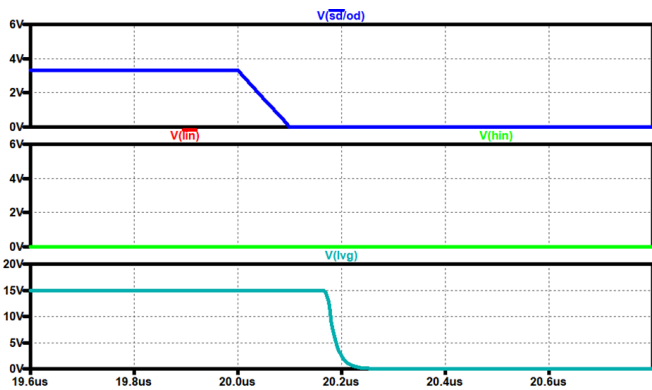
Referred to Data Sheet



Simulation results are following.
Explanatory notes — : simulated

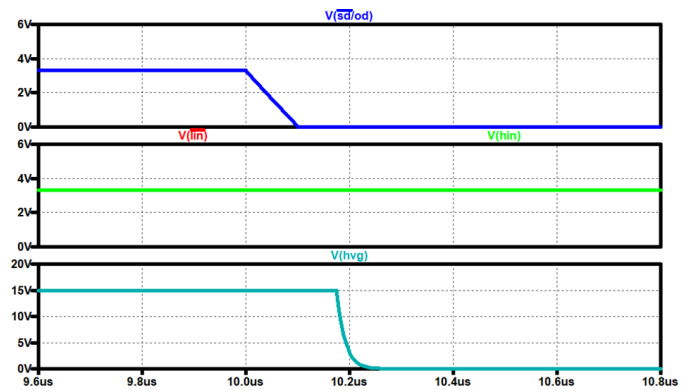
Switching

• Lside



t_{sd}	123 ns
t_f	33.8 ns

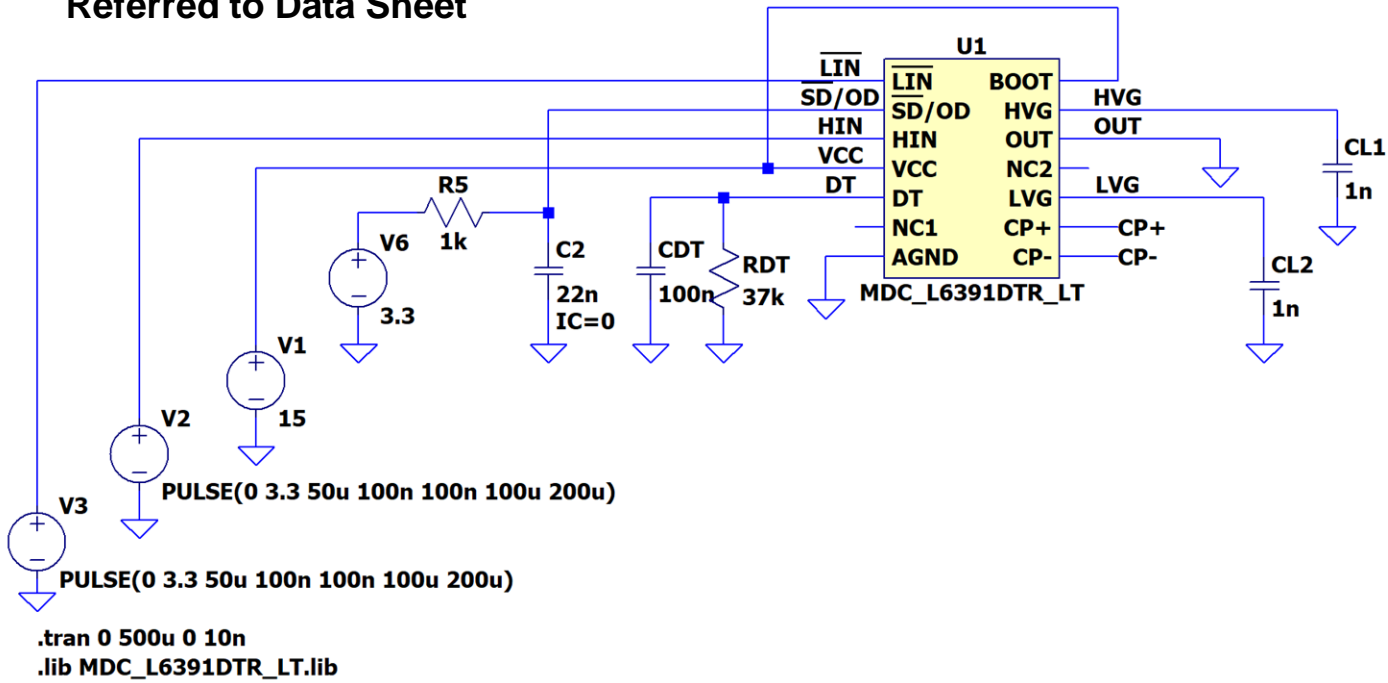
• Hside



t_{on}	127 ns
t_f	35 ns

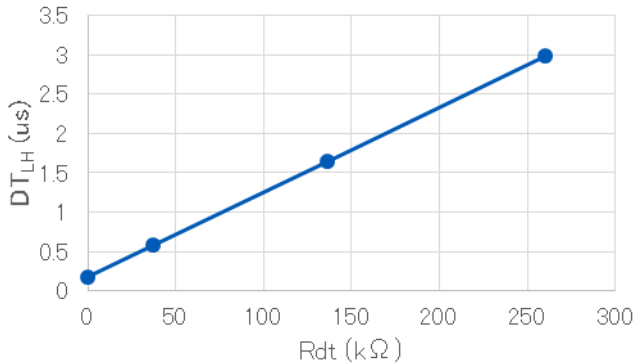
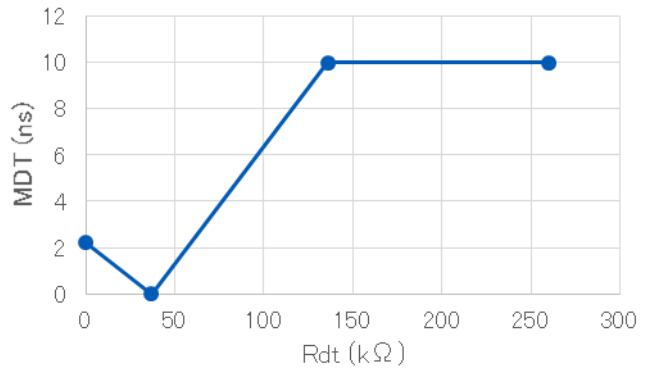
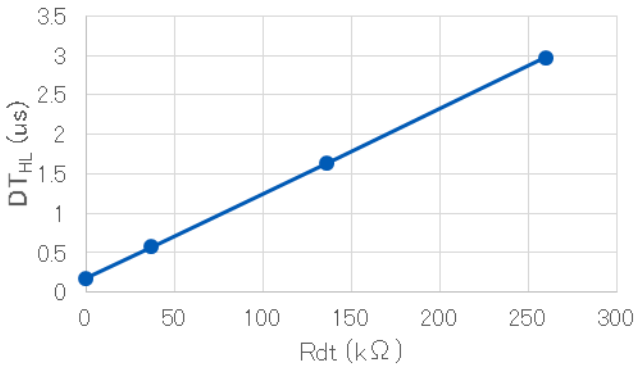
Dead Time Testbench

Referred to Data Sheet



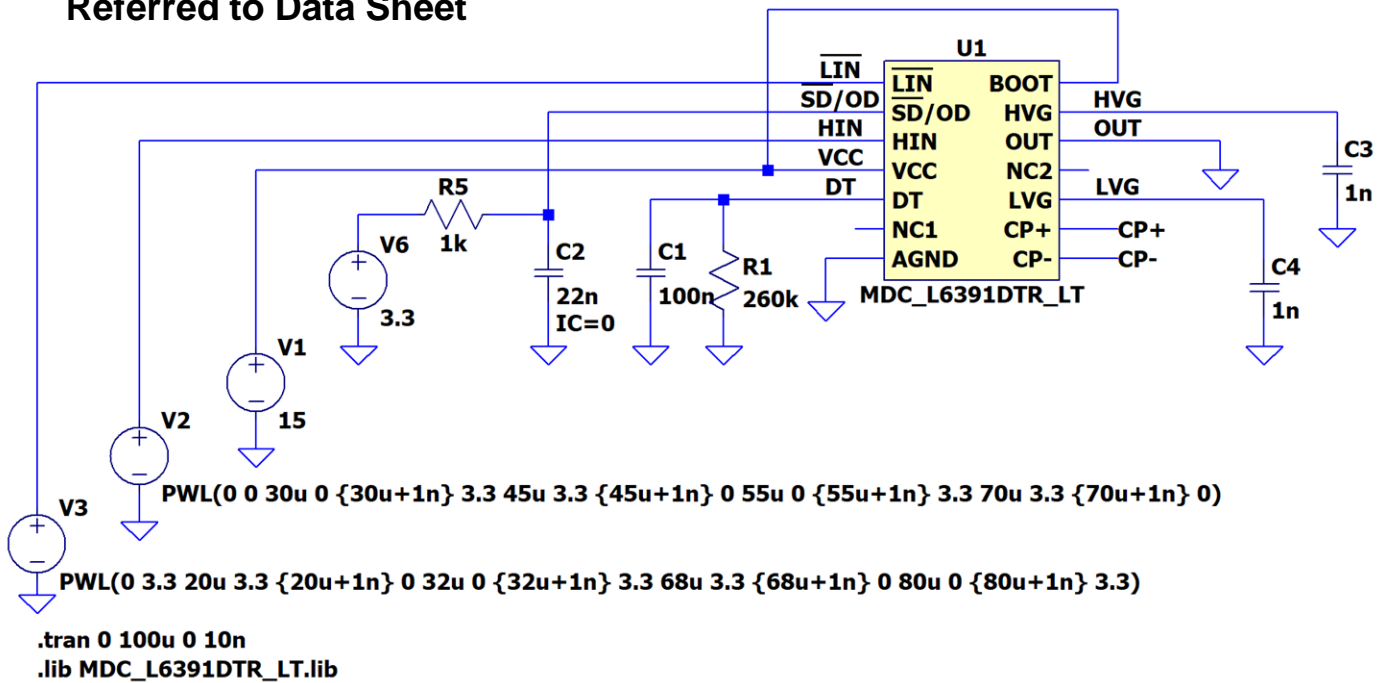
Simulation results are following.
 Explanatory notes — : simulated

Dead Time



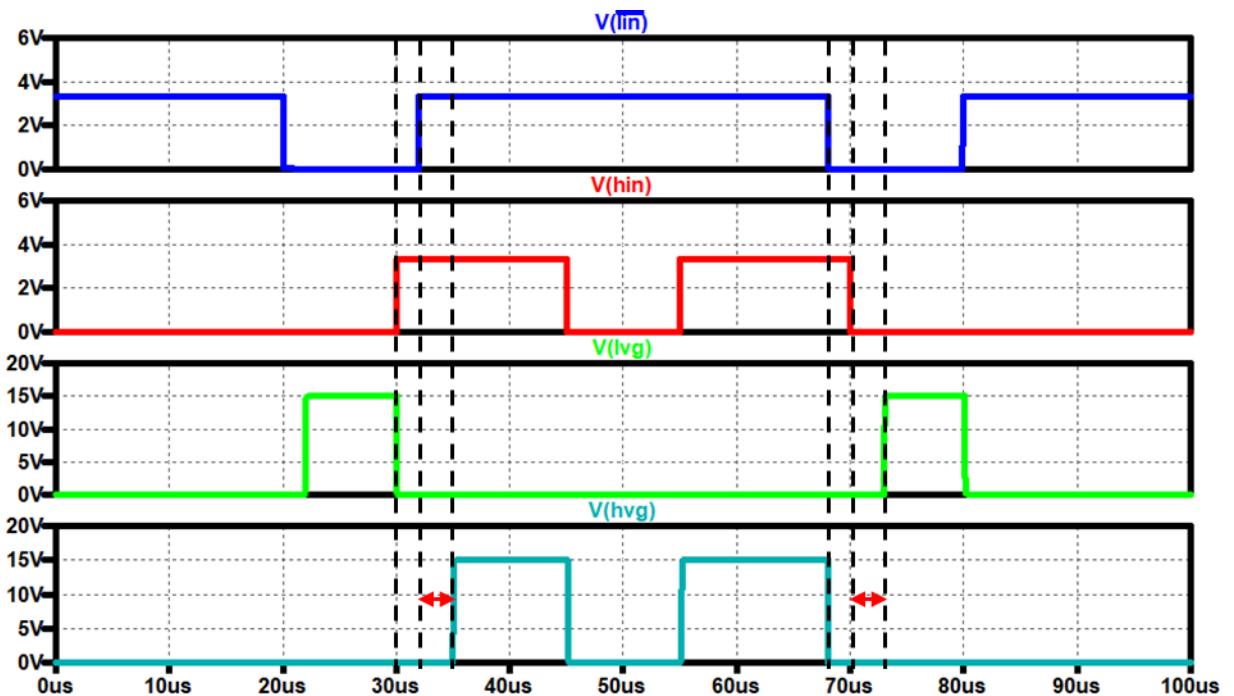
Time Chart① Testbench

Referred to Data Sheet



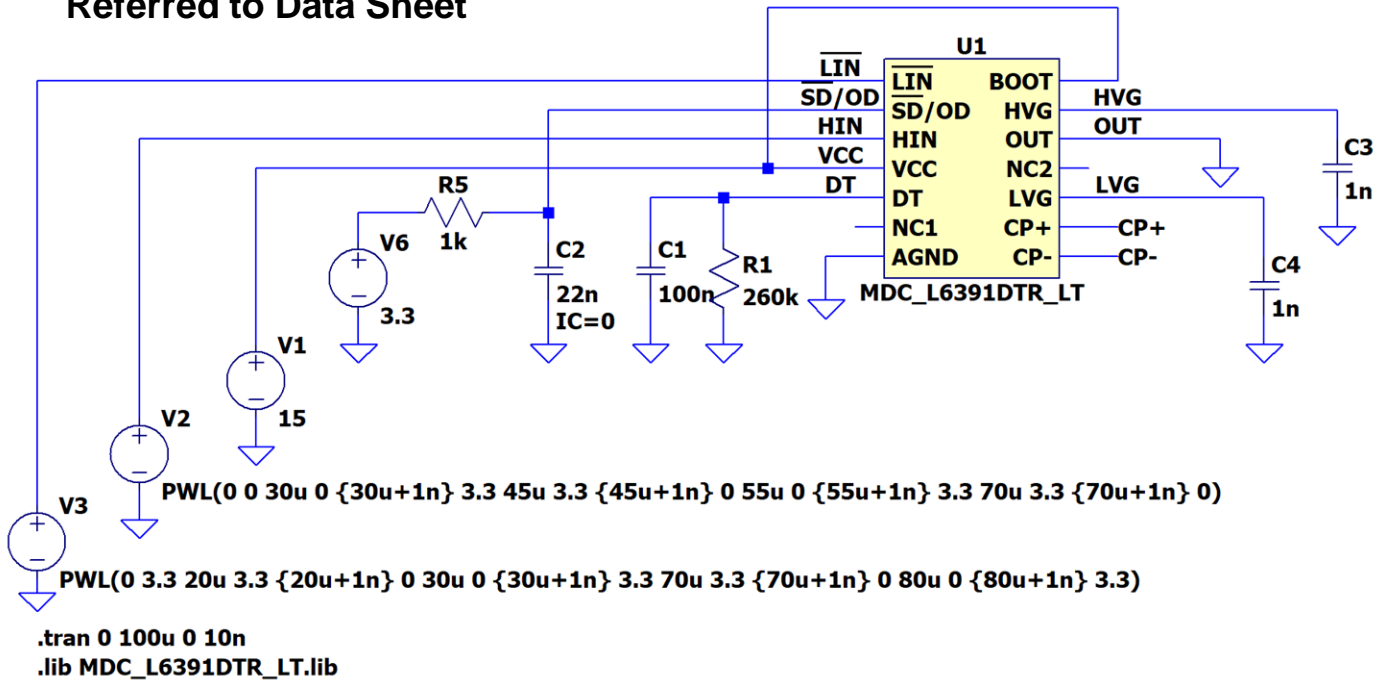
Simulation results are following.
 Explanatory notes — : simulated

Time Chart①



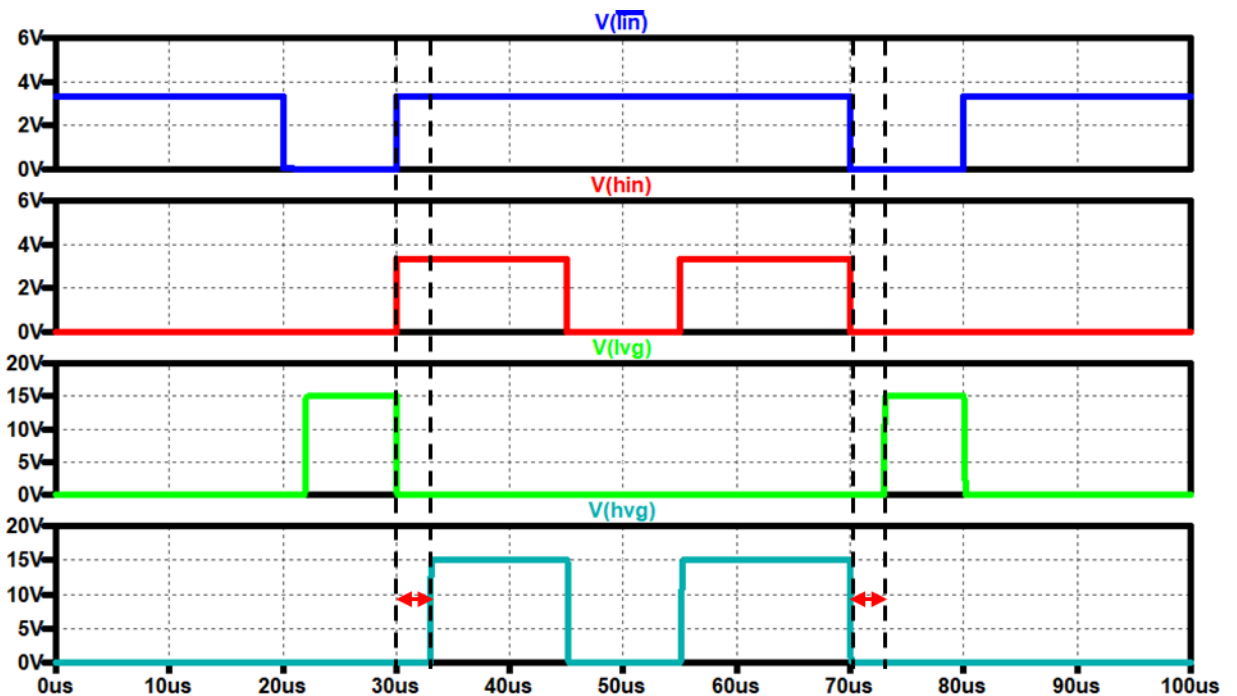
Time Chart② Testbench

Referred to Data Sheet



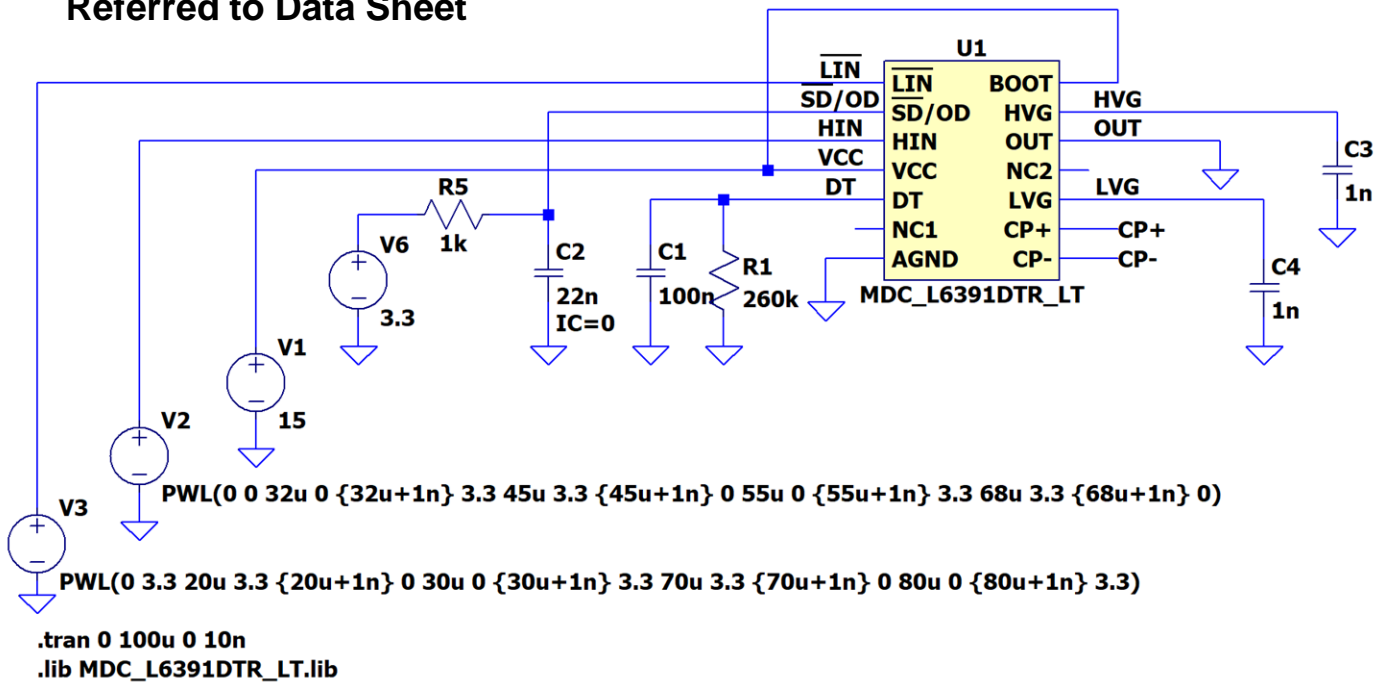
Simulation results are following.
 Explanatory notes — : simulated

Time Chart②



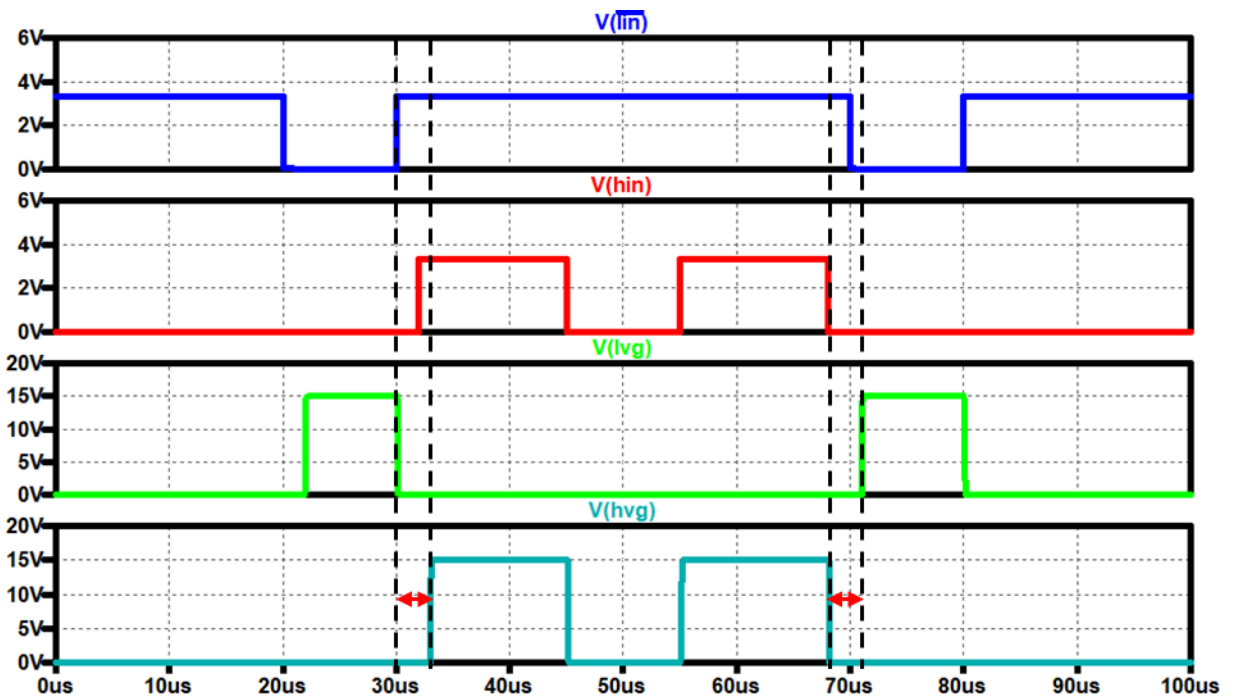
Time Chart③ Testbench

Referred to Data Sheet



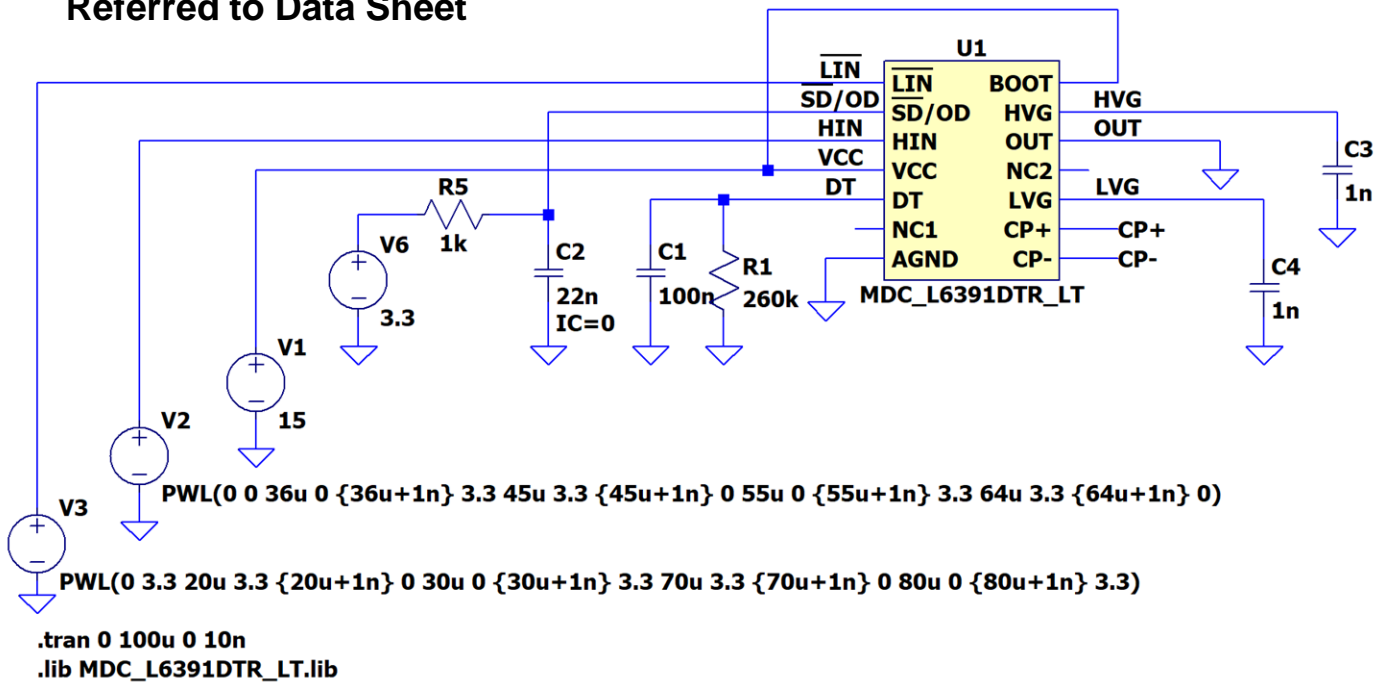
Simulation results are following.
 Explanatory notes — : simulated

Time Chart③



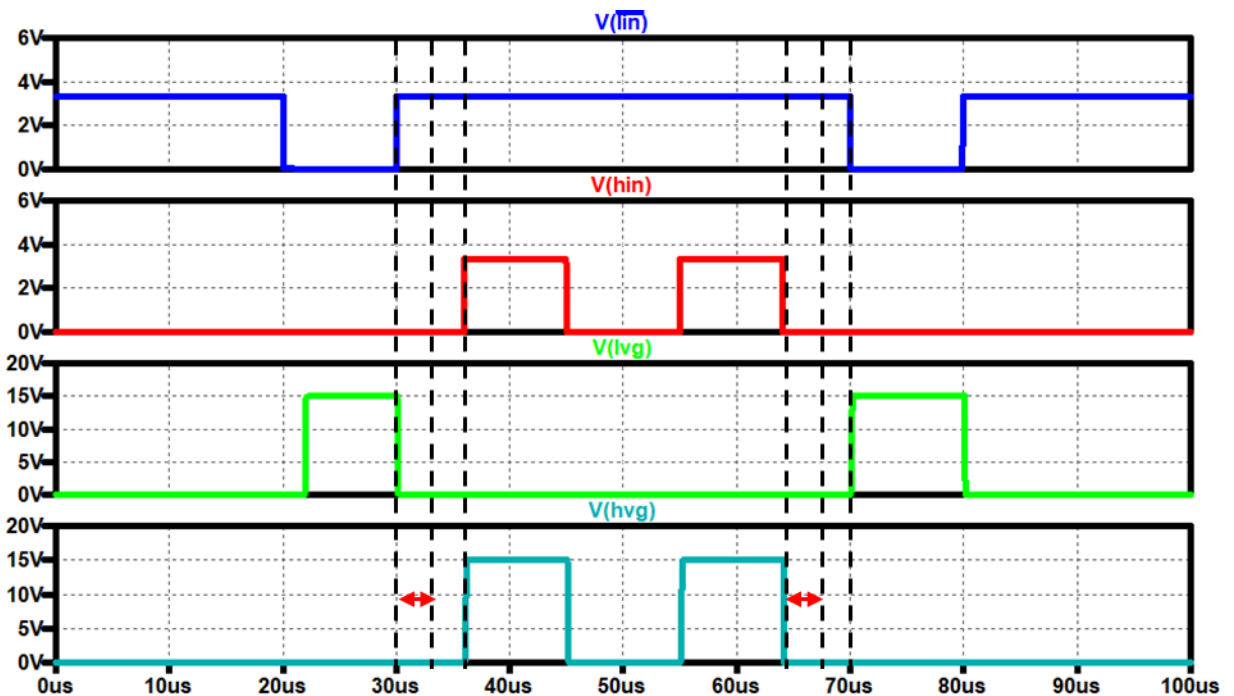
Time Chart④ Testbench

Referred to Data Sheet



Simulation results are following.
 Explanatory notes — : simulated

Time Chart④



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