

LTspice Model

Synchronous Step-Down Converter

Monolithic Power Systems, Inc.

MPM3805GQB-25-Z

Model Information

Model A macro model
Call Name MDC_MPM3805GQB-25-Z_LT
Pin Assign 1:PGND1 2: PGND2 3:NC 4:NC 5:OUT1 6:OUT2 7:VIN 8:PG 9:EN 10:NC 11:AGND 12:OUT_S
File List Model Library MDC_MPM3805GQB-25-Z_LT01.lib
 Model Report MDC_MPM3805GQB-25-Z_LT.pdf (this file)

Verified Simulator Version LTspice XVII
Note

References

The information which was used for modeling is as follow:

- [Data Sheet]
 - Date/Version 3/23/2015 Rev.1.11
 - Product name MPM3805GQB-25-Z
 - Company name Monolithic Power Systems, Inc.
- [Characteristics listed]
 - Characteristics PWM Control
Soft Start
UVLO Protection
EN Function
Soft Start
Current Limit
Load Regulation

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

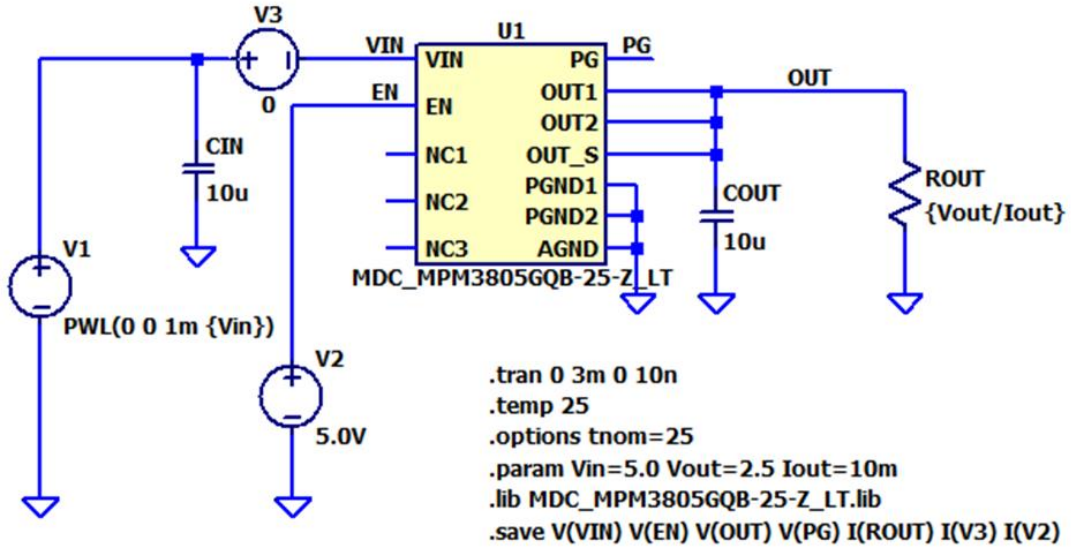
Switching Regulator

○ : Implemented
× : Not Implemented
— : Not applicable

Model Functions Table
RANK=2

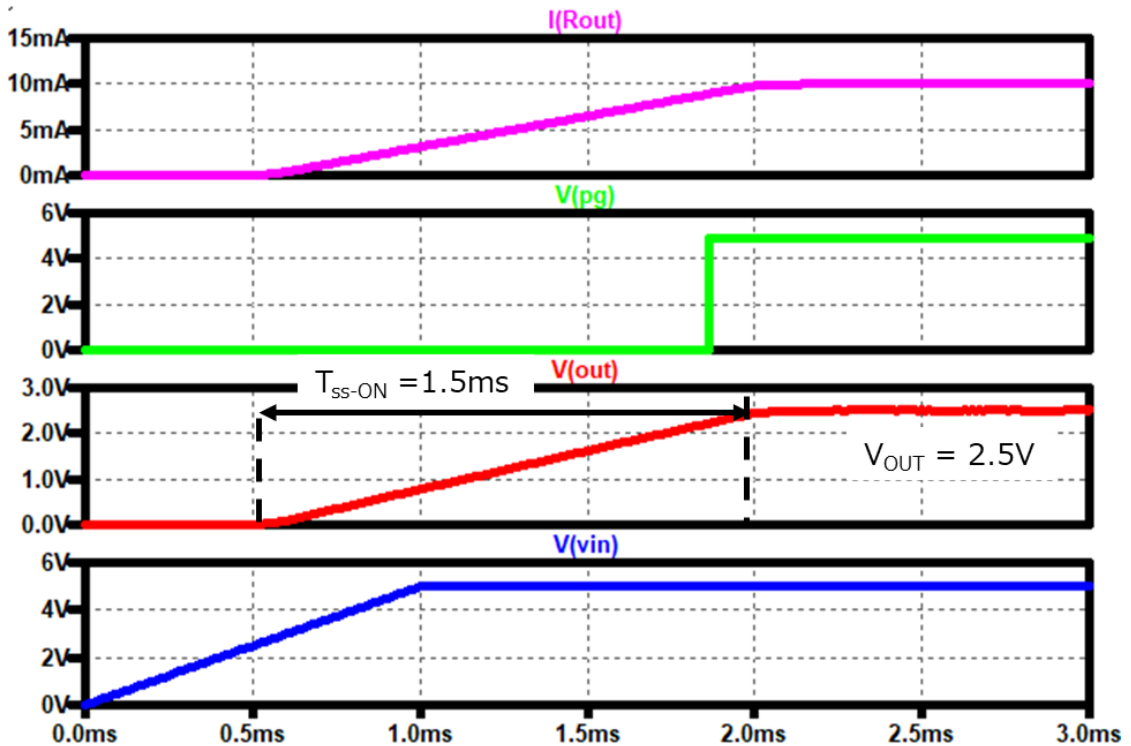
Functions	RANK	Implemented
Control Method(PWM,PFM)	1	○
Enable Function	1	○
Soft Start	1	○
Line Regulation	1	—
Load Regulation	1	○
Synchronous External Oscillation	1	—
UVLO	1	○
Line Transient	2	—
Load Transient	2	—
Light Load Current Mode	2	○
Spread Spectrum	2	—
Over Current Protection	2	○
Over Voltage Protection	2	—
Forard/Flyback Other Device in Circuit	3	—
Brown IN/OUT Function	—	—
ZT Pin OVP Function	—	—

V_{OUT} / Soft start Testbench

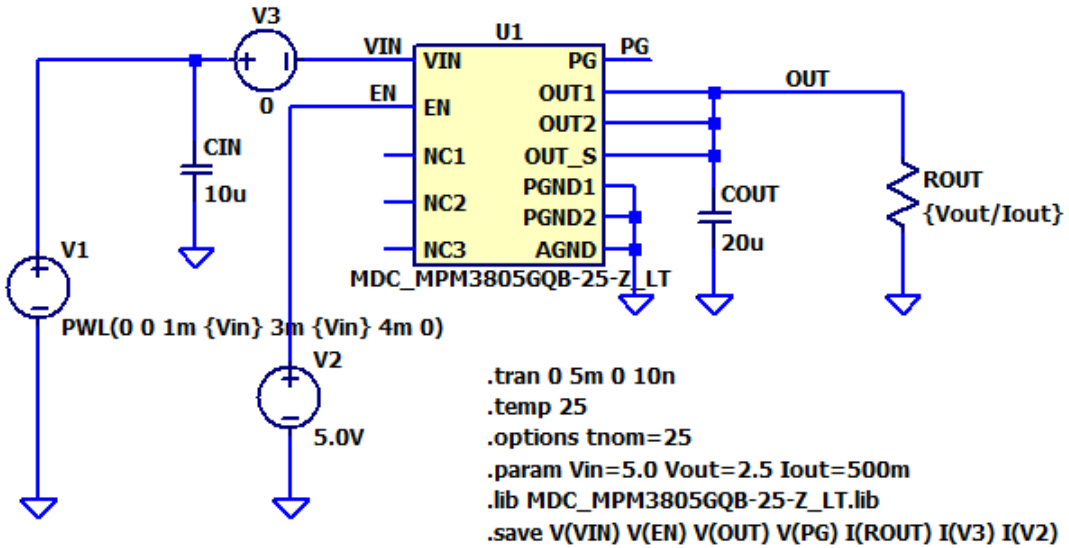


Simulation results are following.
 Explanatory notes — : simulated

V_{OUT} / Soft start

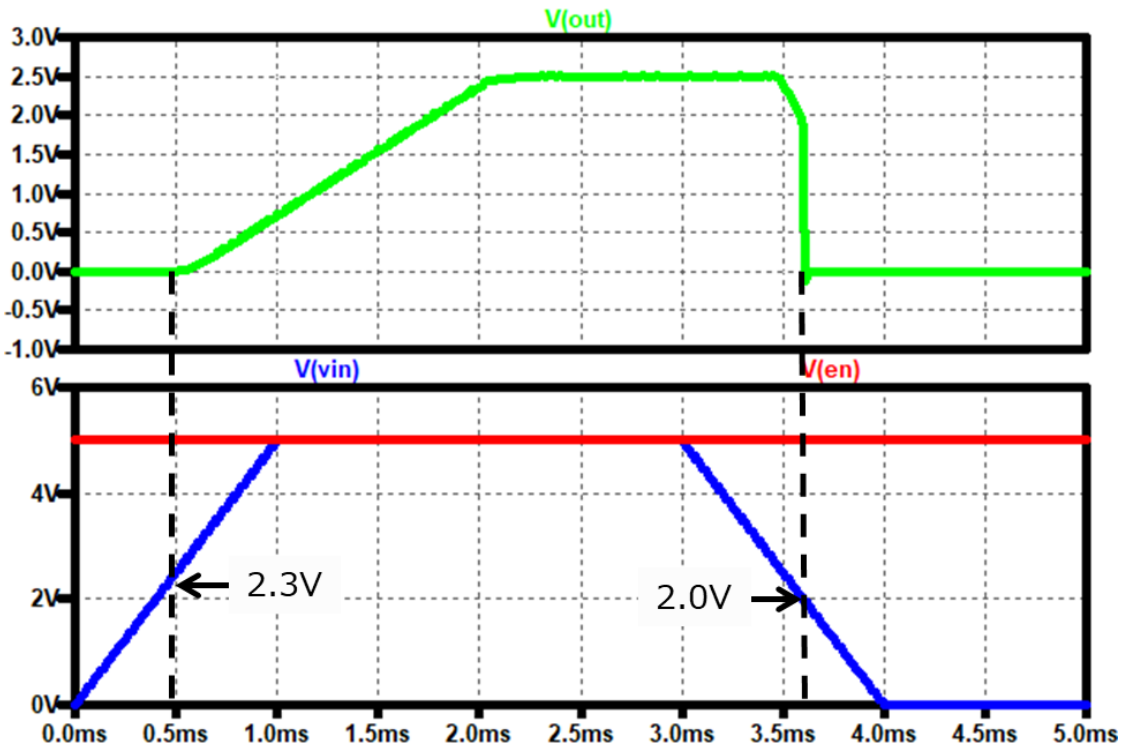


UVLO Testbench

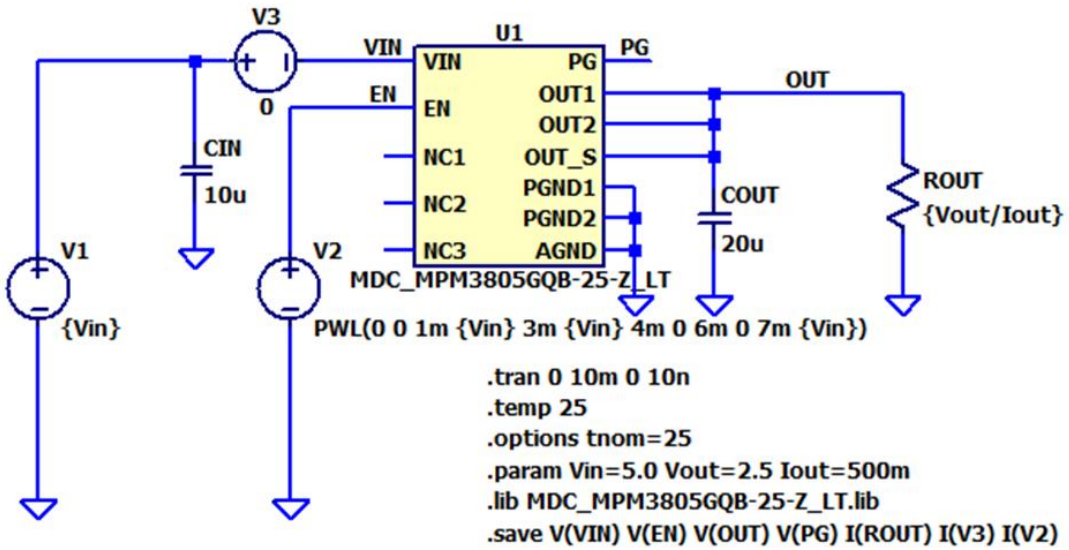


Simulation results are following.
 Explanatory notes — : simulated

UVLO

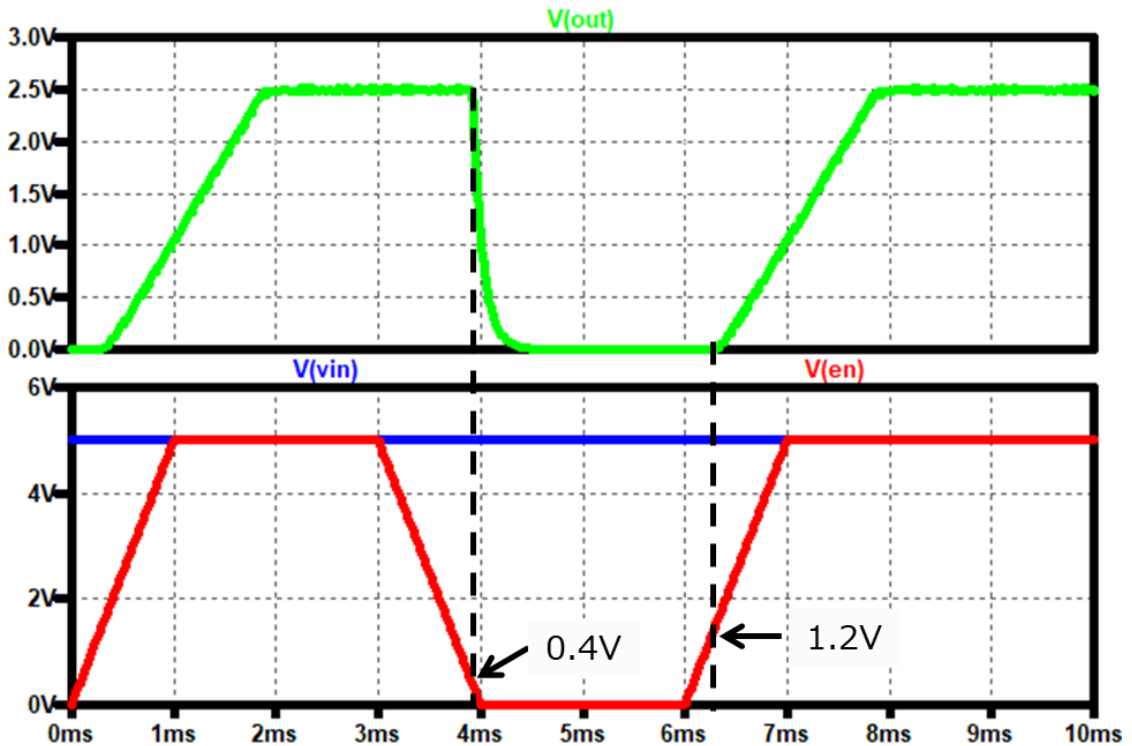


EN Testbench

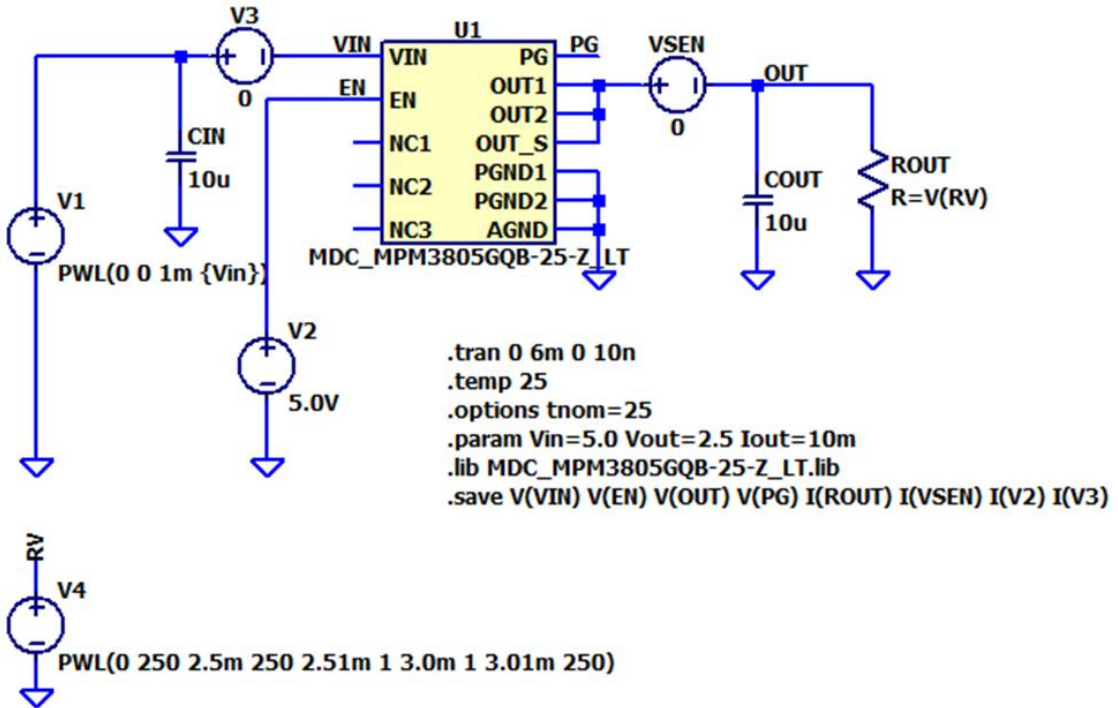


Simulation results are following.
 Explanatory notes — : simulated

EN

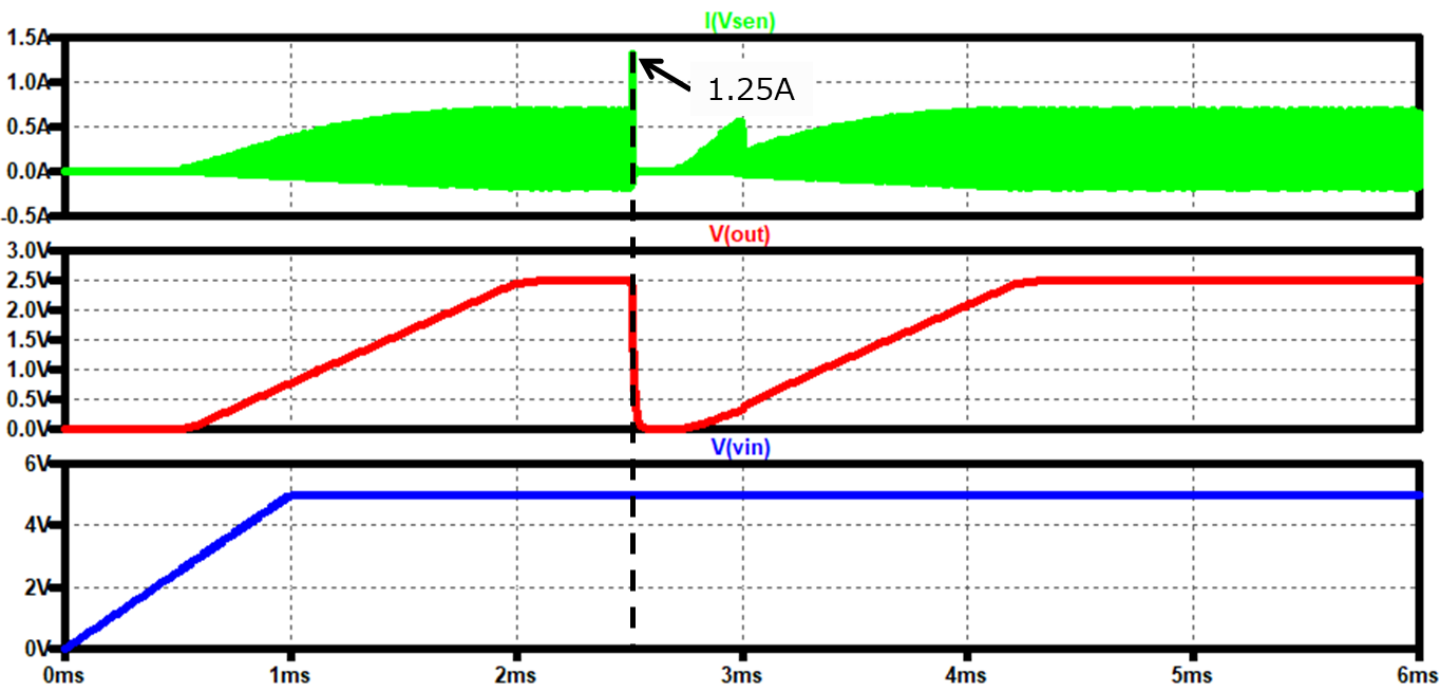


Current Limit Testbench

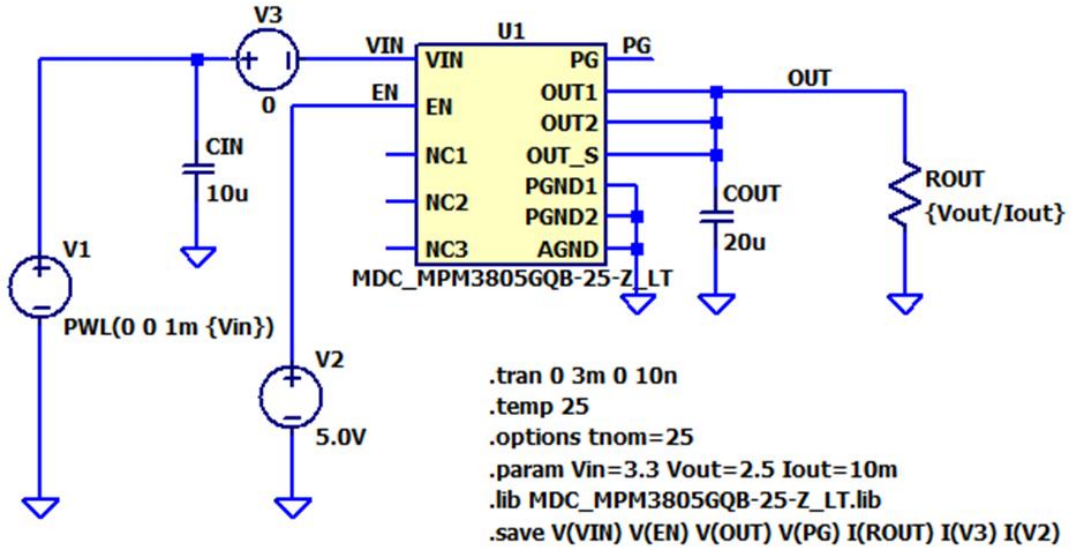


Simulation results are following.
 Explanatory notes — : simulated

Current Limit

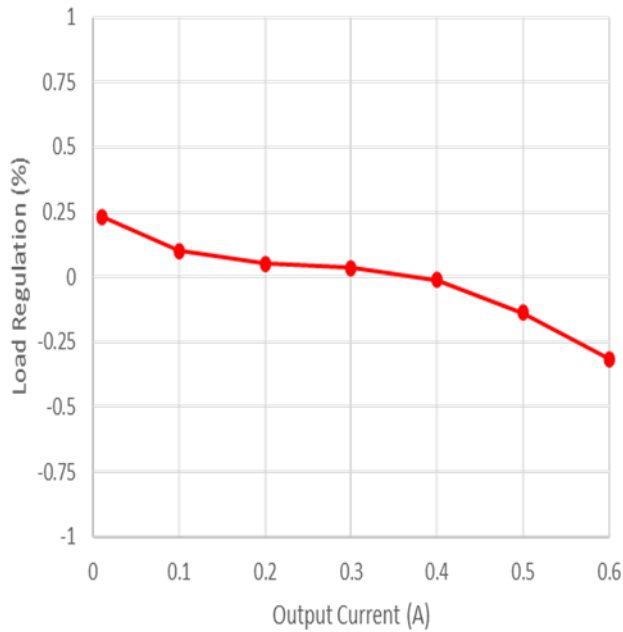


Load Regulation (Vin = 3.3V) Testbench

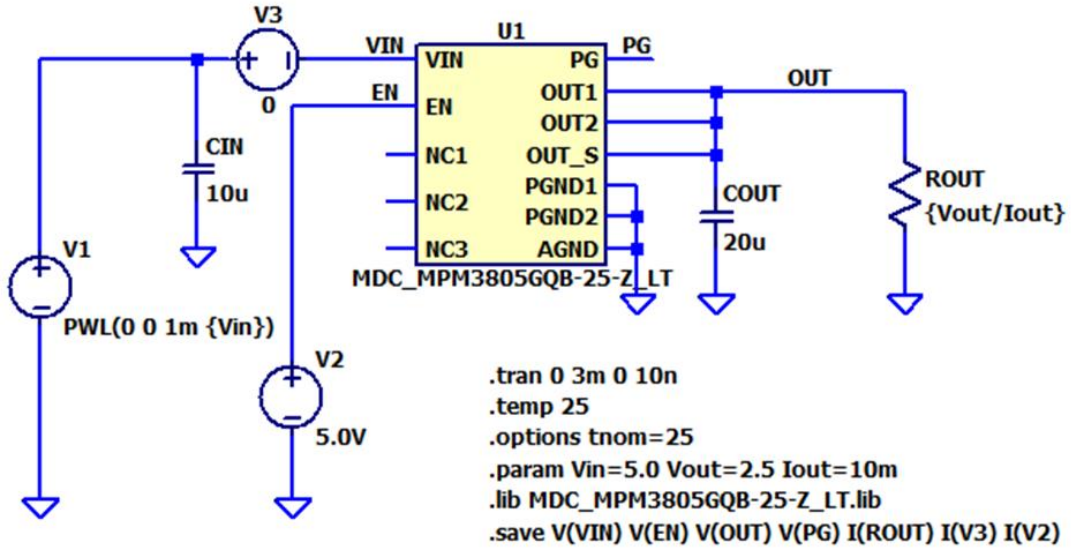


Simulation results are following.
 Explanatory notes — : simulated

Load Regulation (Vin = 3.3V)

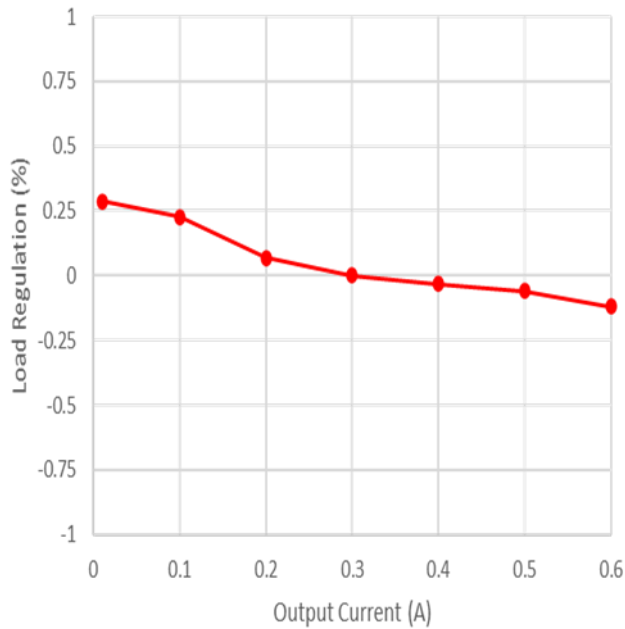


Load Regulation (Vin = 5.0V) Testbench



Simulation results are following.
 Explanatory notes — : simulated

Load Regulation (Vin = 5.0V)



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