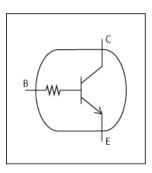


PSpice Model BRT (Bias Resistor Transistor) TOSHIBA RN1410



Model Information

ModelA macro model based on Mextram modelCall NameMDC_RN1410_PSPin Assign1:C 2:B 3:EFile ListModel Library
Model ReportMDC_RN1410_PS02.lib
MDC_RN1410_PS.pdf (this file)

Verified Simulator Version Note

PSpice version 16.6

References

The information which was used for modeling is as follow:

[Data Sheet] • Date/Version • Product name • Company name

Characteristics

Unknown RN1410 Toshiba Corporation IcVi[OFF],IcVi[ON],hFEIc[Temp],Vce(sat)Ic[Temp]

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

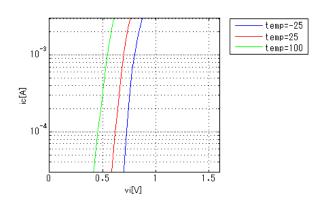
Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
Temperature	-55	to	150	deg C



Simulation results are following. Explanatory notes — : simulated

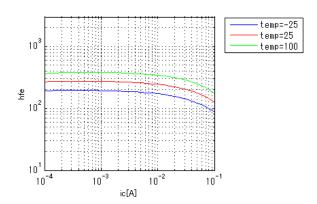
lcVi[OFF]

Vce = 5V



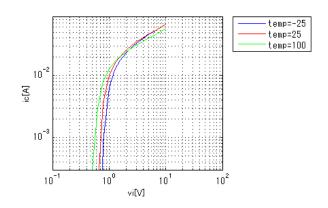
hFElc[Temp]

Vce = 5V



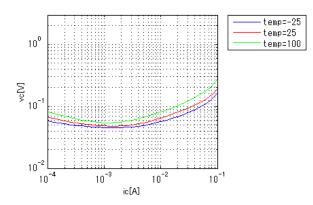
lcVi[ON]





Vce(sat)lc[Temp]

IC/IB = 20





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