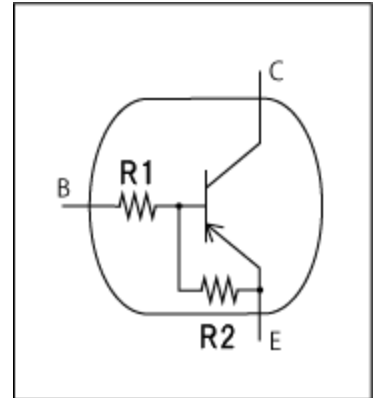


LTspice Model

BRT (Bias Resistor Transistor)

Isahaya

RT1N141M



Model Information

Model A macro model based on Gummel-Poon model
Call Name MDC_RT1N141M_LT
Pin Assign 1:B 2:E 3:C
File List Model Library MDC_RT1N141M_LT02.lib
 Model Report MDC_RT1N141M_LT.pdf (this file)

Verified Simulator Version LTspice version XVII
Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2016/11
- Product name RT1N141M
- Company name Isahaya Electronics Corporation
- Characteristics $hFEI_c[Temp]$, $V_{ionI_c[Temp]}$, $I_{cVioff[Temp]}$, $V_{ce(sat)I_c[Temp]}$, $f_{Tle[Vce]}$

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
R1	10,000	to	10,000	ohm
R2	10,000	to	10,000	ohm
Temperature	-55	to	150	deg C

BRT

○ : Implemented
 × : Not Implemented
 — : Not applicable

Model Functions Table

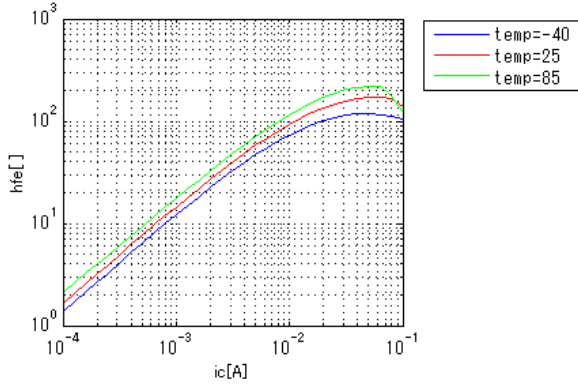
RANK=1

Functions	RANK	Implemented
VIN(on)-Iout(Temp)	1	○
Iout-VIN(off)(Temp)	1	○
hFE-Ic(Temp)	1	○
Vce(sat)-Ic(Temp)	1	○
Capacitance	1	—
Transition Frequency	1	○
Switching(Typ.)	1	—

Simulation results are following.
 Explanatory notes — : simulated

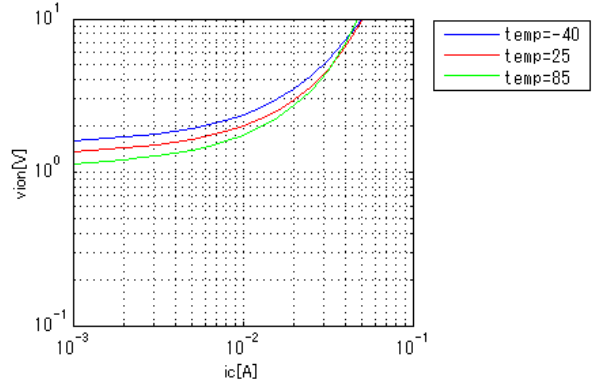
hFEIc[Temp]

Vce = 5V



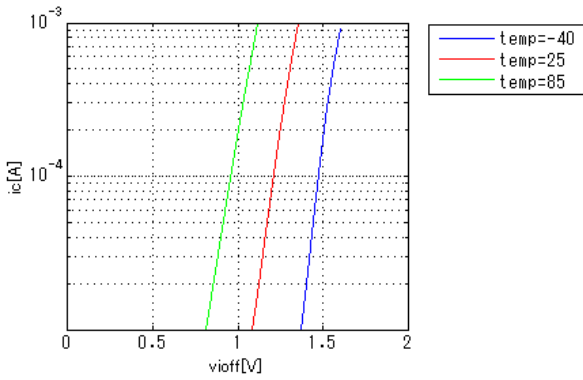
VionIc[Temp]

Vce = 0.2V



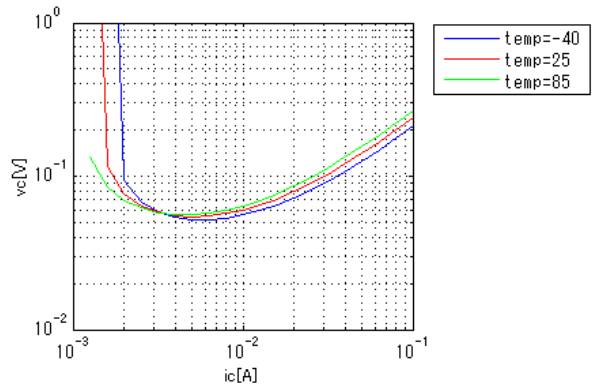
IcVioff[Temp]

Vce = 5V



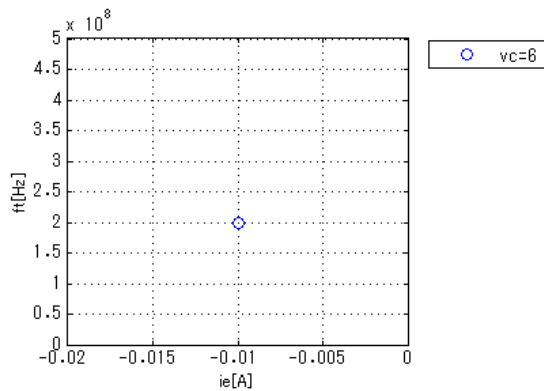
Vce(sat)Ic[Temp]

IC/IB = 20



fTle[Vce]

Freq = 20000000Hz



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