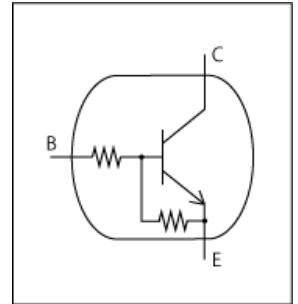


# LTspice Model

## BRT (Bias Resistor Transistor)

### Isahaya

### RT1N242M



### Model Information

**Model** A macro model based on Mextram 504 model  
**Call Name** MDC\_RT1N242M\_LT  
**Pin Assign** 1:B 2:E 3:C  
**File List** Model Library MDC\_RT1N242M\_LT01.lib  
 Model Report MDC\_RT1N242M\_LT.pdf (this file)

**Verified Simulator Version** LTspice version XVII  
**Note**

### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2016/11
- Product name RT1N242M
- Company name Isahaya Electronics Corporation
- Characteristics hFEIc[Temp], Vi(ON)Ic[Temp], IcVi(OFF)[Temp], Vce(sat)Ic[Temp], fT Ic[Vce]

### Simulation Range

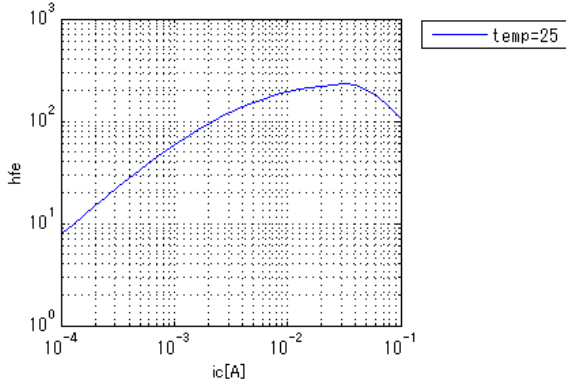
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
Collector current (DC)	0	to	100m	A
Temperature	-55	to	150	deg C

Simulation results are following.  
 Explanatory notes — : simulated

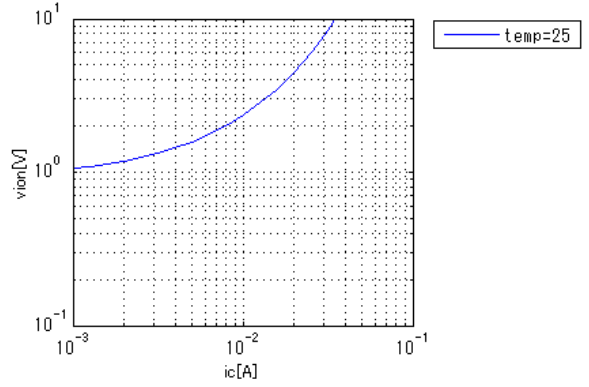
**hFEIc[Temp]**

Vce = 5V



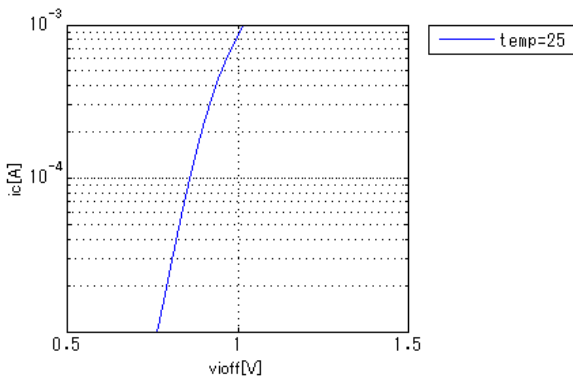
**Vi(ON)Ic[Temp]**

Vce = 0.2V



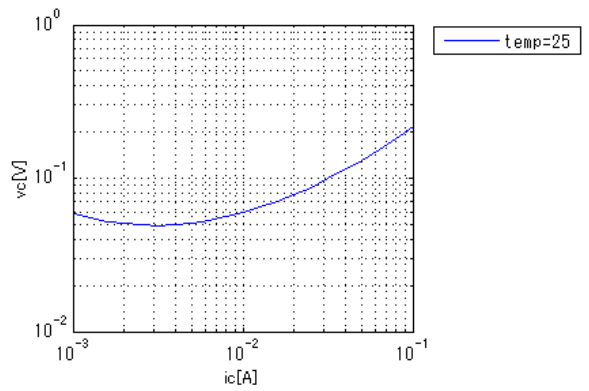
**IcVi(OFF)[Temp]**

Vce = 5V

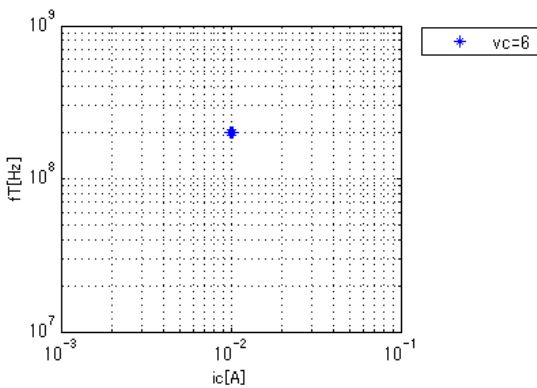


**Vce(sat)Ic[Temp]**

IC/IB = 20



**fT[Ic[Vce]]**



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