

# PSpice Model

## Resistor-equipped Double Transistor

### Nexperia

### PUMD3

#### Model Information

<b>Model</b>	A macro model
<b>Call Name</b>	MDC_PUMD3_PS
<b>Pin Assign</b>	1:GND1 2:I1 3:O2 4:GND2 5:I2 6:O1
<b>File List</b>	Model Library MDC_PUMD3_PS.lib Model Report MDC_PUMD3_PS.pdf(this file)
<b>Verified Simulator Version</b>	PSpice v17.2

#### Note

#### References

The information which was used for modeling is as follow:

##### [Data Sheet]

- Date/Version 1 July 2022
- Product name PUMD3
- Company name Nexperia B.V.

##### [Characteristics listed]

- Characteristics VCEsat-IC[temp]  
IC-VCE[IB]  
hFE-IC[temp]  
VI(on)-IC[temp]  
VI(off)-IC[temp]  
Cc-Vcb  
fT-IC

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Temperature	25	deg C

○ : Implemented  
 × : Not Implemented  
 — : Not applicable

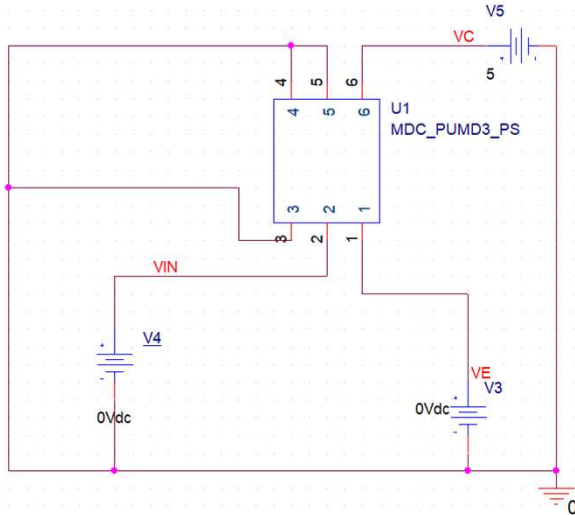
**Model Functions Table**

		RANK=1	
Functions	RANK	Implemented	
VIN(on)-Iout(Temp)	1	○	
Iout-VIN(off)(Temp)	1	○	
Iout-Vo-Iin	1	○	
DC_Current_Gain-Iout	1	○	
VOUT(on)-Iout(Temp)	1	—	
VOUT(sat)-Iin(Temp)	1	○	
Capacitance	1	○	
Transition Frequency	1	○	
Switching(Typ.)	1	—	

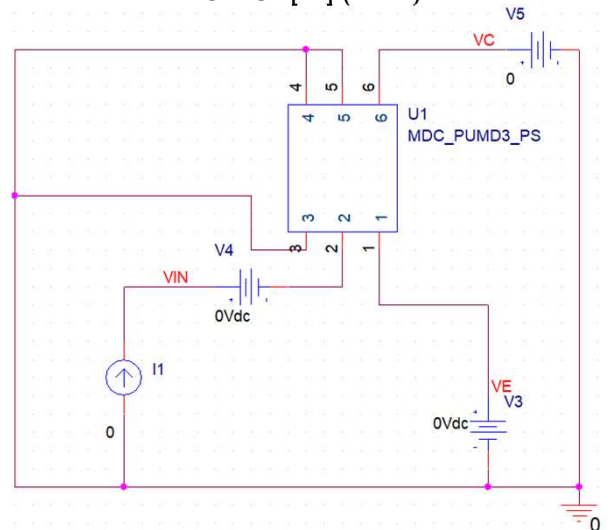
hFE-IC[temp](NPN) , IC-VCE[IB](NPN) Testbench

Referred to Data Sheet

hFE-IC[temp] (NPN)



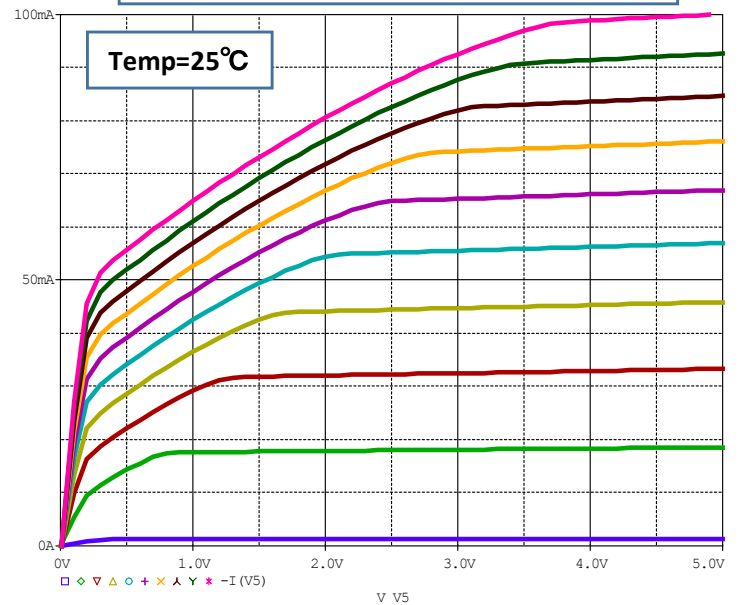
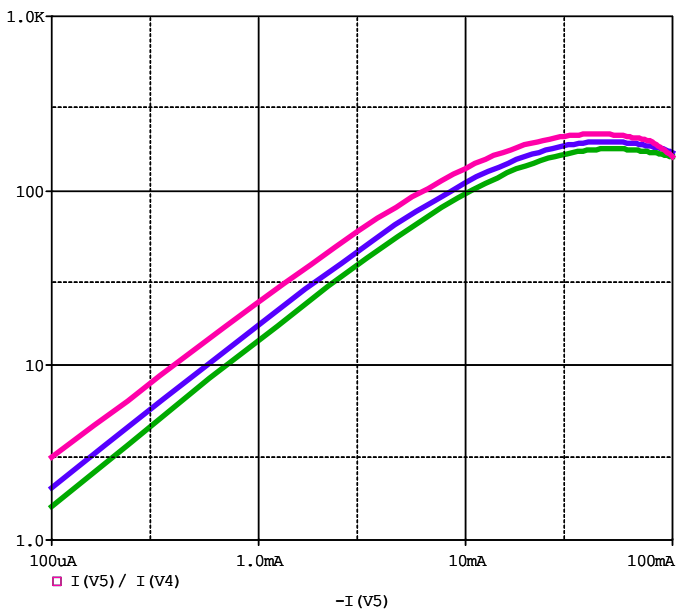
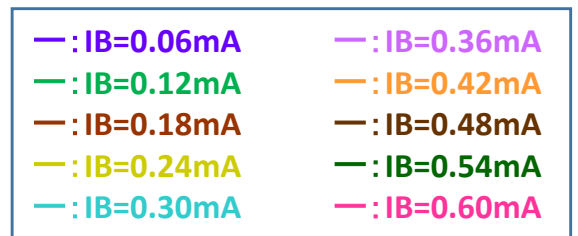
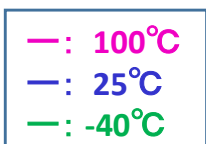
IC-VCE[IB] (NPN)



Simulation results are following.  
Explanatory notes — : simulated

hFE-IC[temp] (NPN)

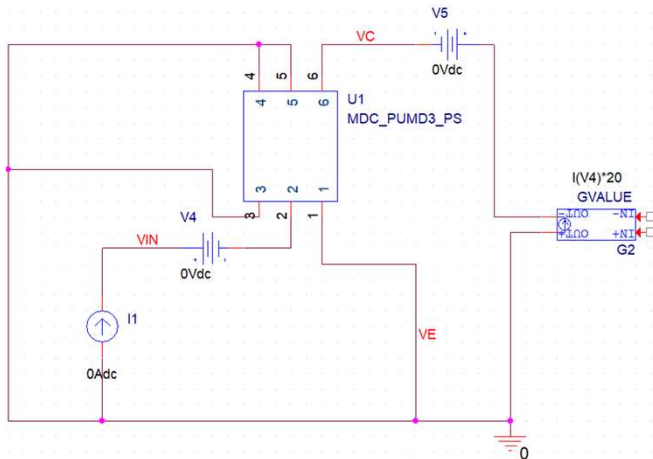
IC-VCE[IB] (NPN)



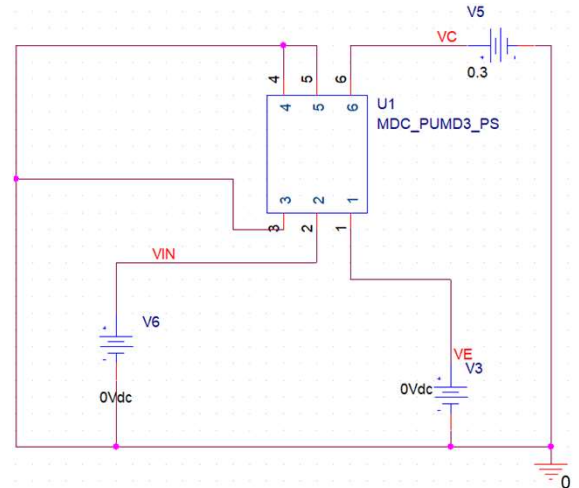
VCEsat-IC[temp](NPN), VI(on)-IC[temp](NPN) Testbench

Referred to Data Sheet

VCEsat-IC[temp] (NPN)



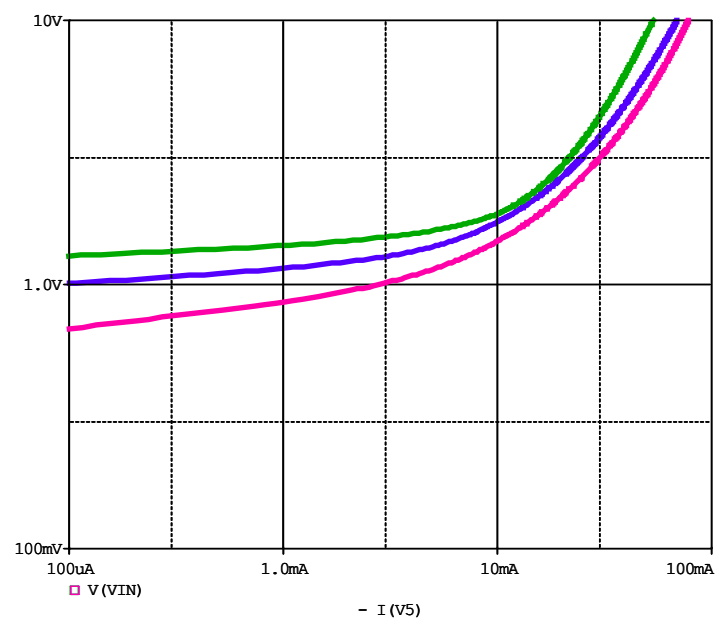
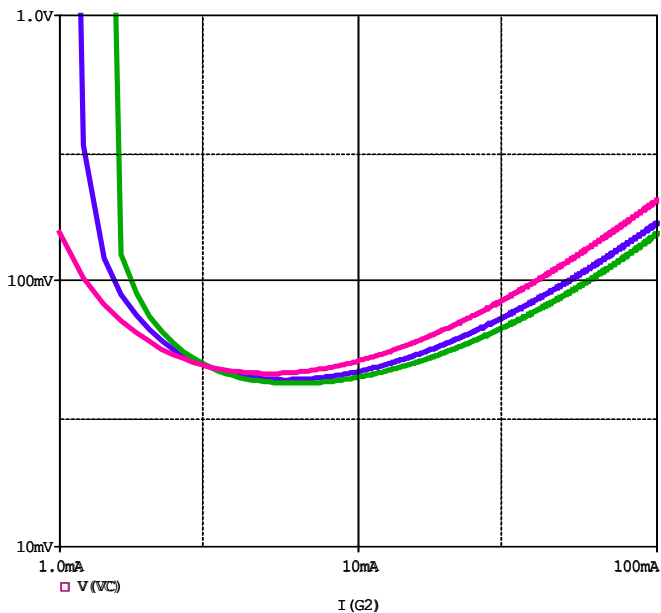
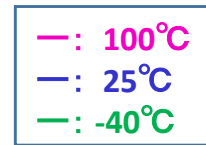
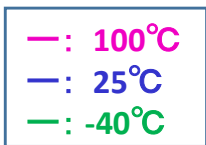
VI(on)-IC[temp] (NPN)



Simulation results are following.  
Explanatory notes — : simulated

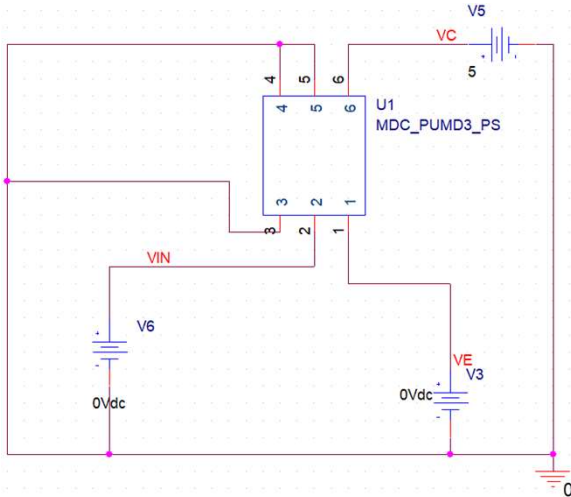
VCEsat-IC[temp] (NPN)

VI(on)-IC[temp] (NPN)

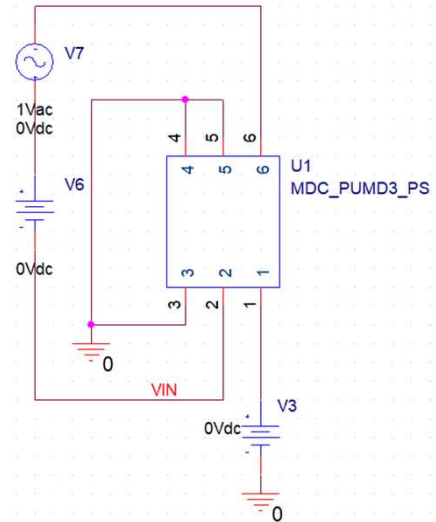


**VI(off)-IC[temp](NPN), Cc-Vcb(NPN) Testbench  
Referred to Data Sheet**

VI(off)-IC[temp] (NPN)



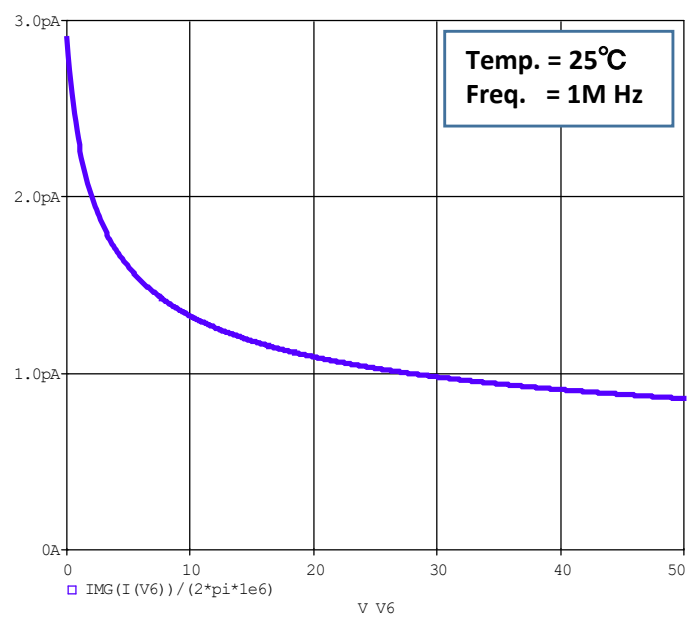
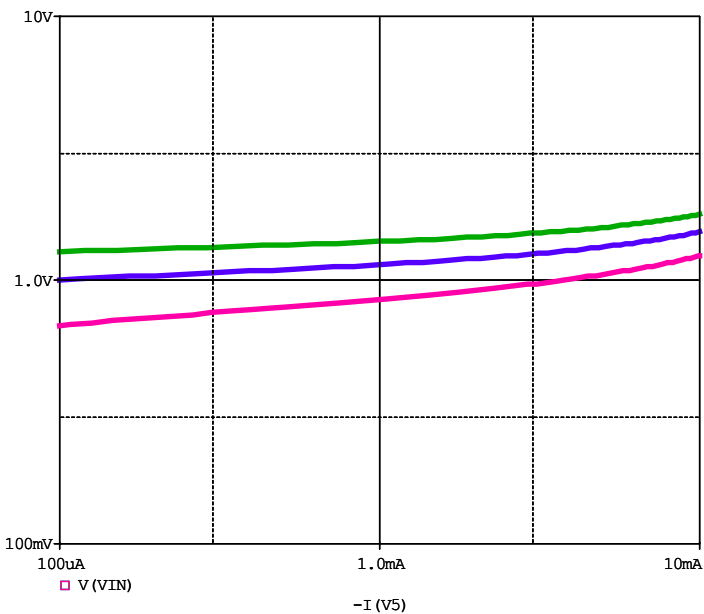
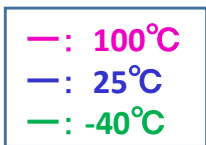
Cc-Vcb (NPN)



Simulation results are following.  
Explanatory notes — : simulated

VI(off)-IC[temp] (NPN)

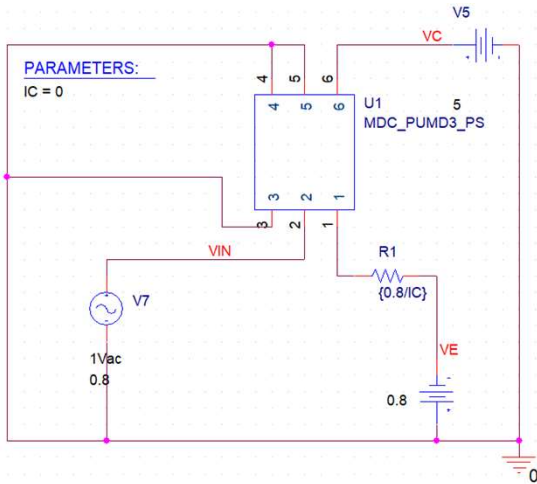
Cc-Vcb (NPN)



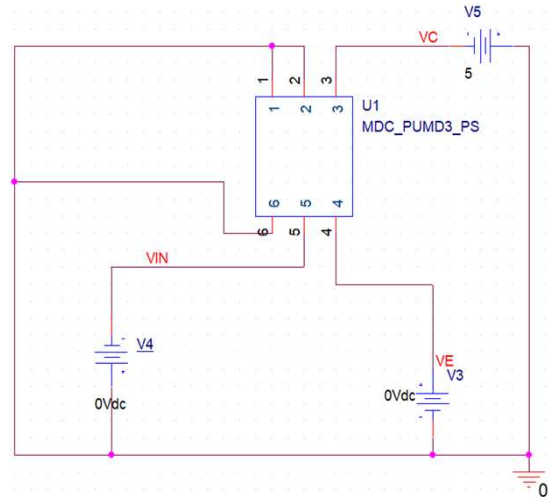
ft-IC(NPN), hFE-IC[temp](PNP) Testbench

Referred to Data Sheet

ft-IC (NPN)

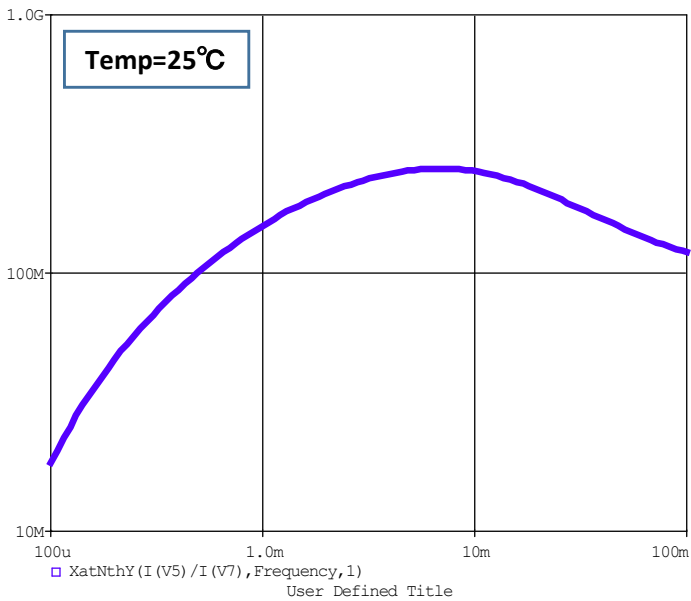


hFE-IC[temp] (PNP)

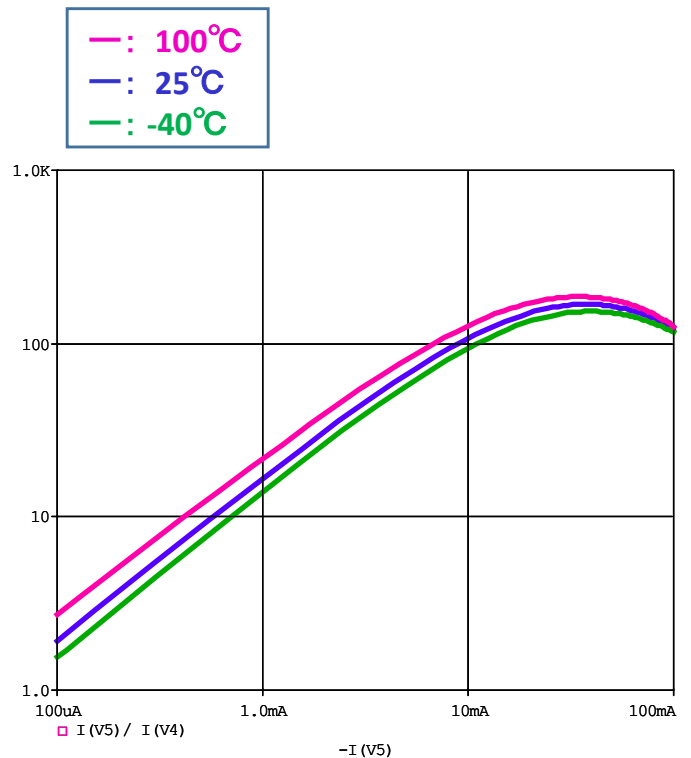


Simulation results are following.  
Explanatory notes — : simulated

ft-IC (NPN)



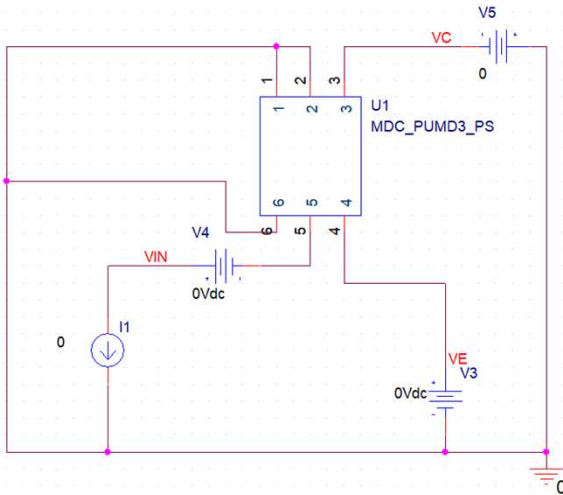
hFE-IC[temp] (PNP)



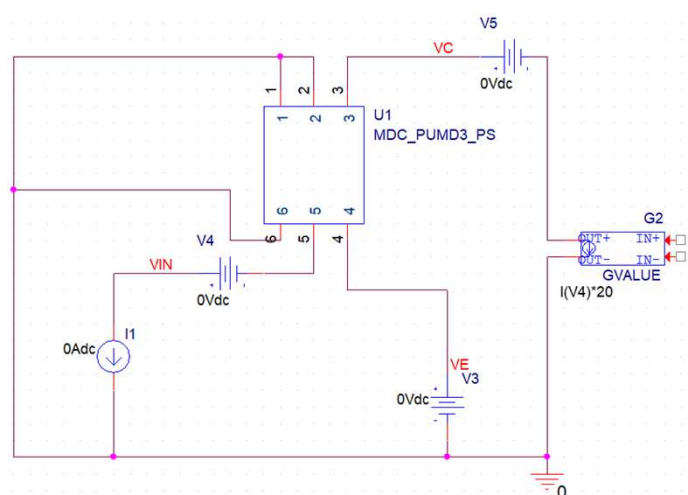
IC-VCE[IB](PNP), VCEsat-IC[temp](PNP) Testbench

Referred to Data Sheet

IC-VCE[IB](PNP)

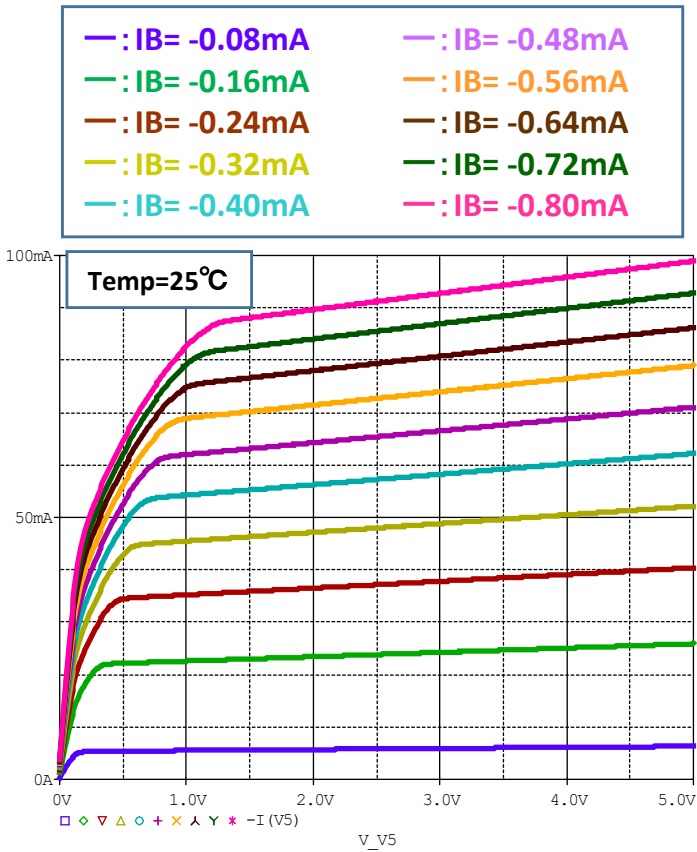


VCEsat-IC[temp](PNP)

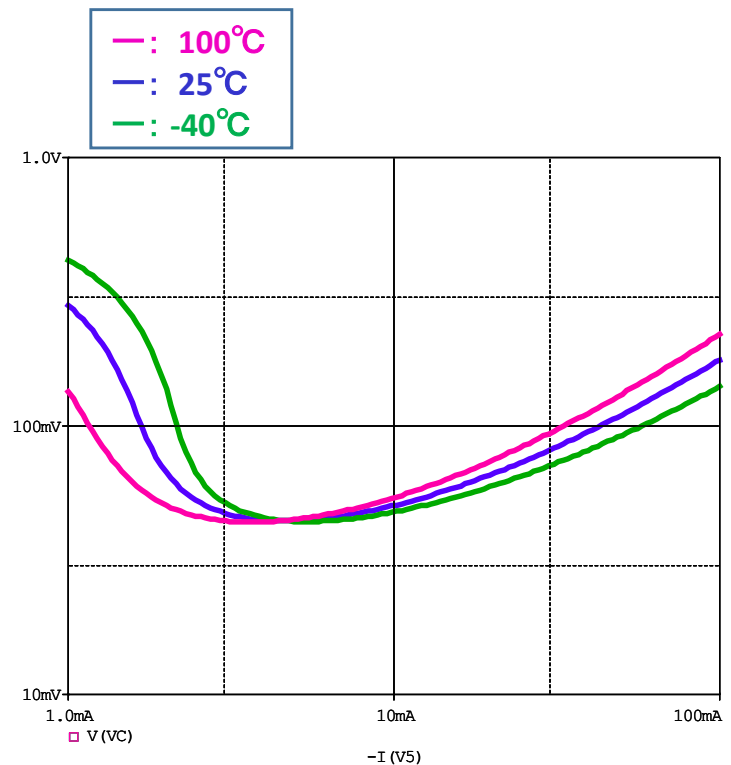


Simulation results are following.  
Explanatory notes — : simulated

IC-VCE[IB](PNP)



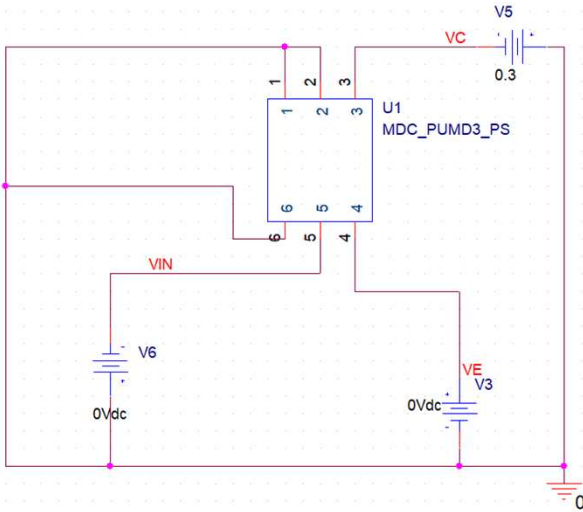
VCEsat-IC[temp](PNP)



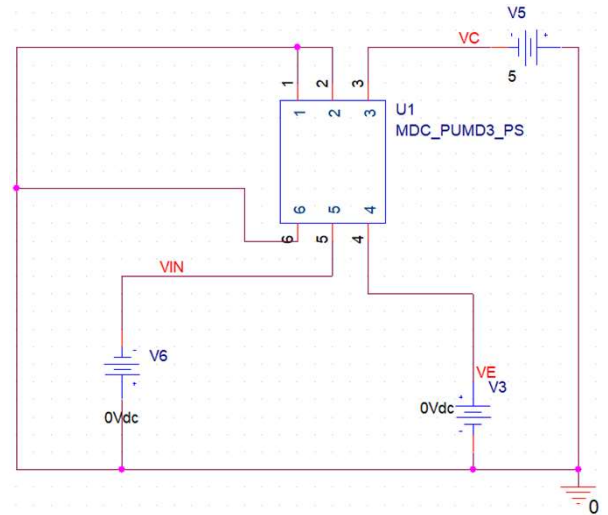
VI(on)-IC[temp](PNP), VI(off)-IC[temp](PNP) Testbench

Referred to Data Sheet

VI(on)-IC[temp](PNP)



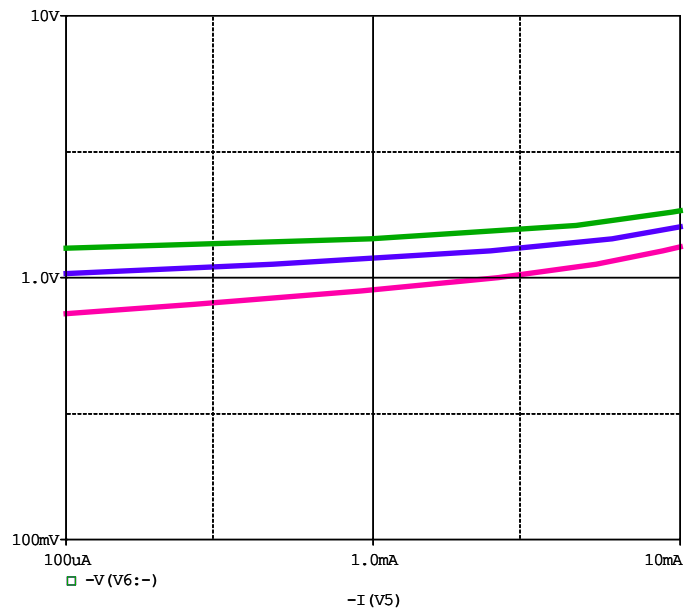
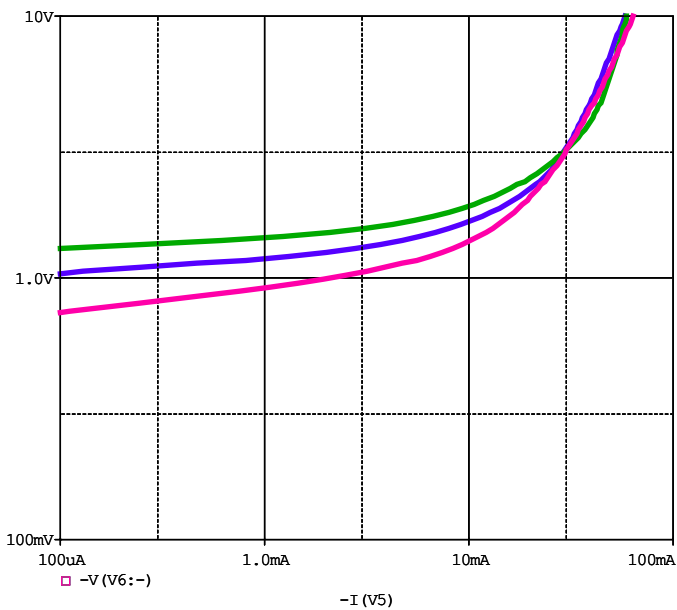
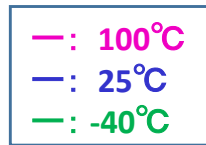
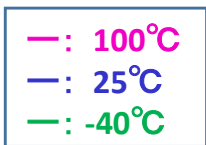
VI(off)-IC[temp](PNP)



Simulation results are following.  
Explanatory notes — : simulated

VI(on)-IC[temp](PNP)

VI(off)-IC[temp](PNP)

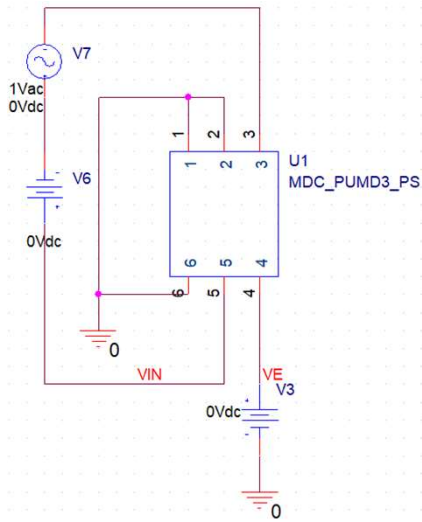




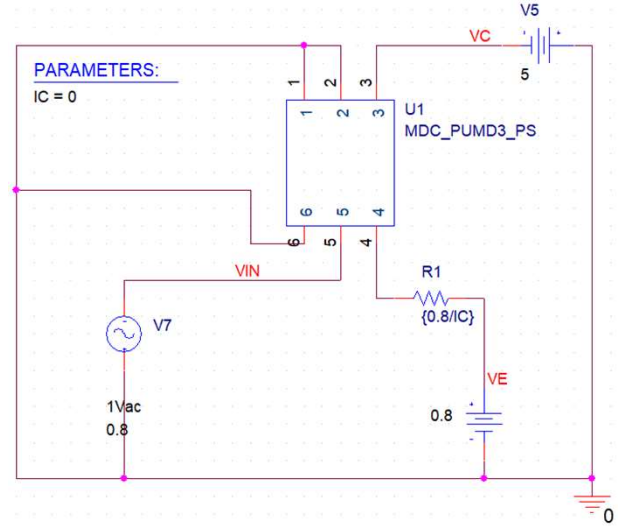
Cc-Vbc(PNP), fT-IC(PNP) Testbench

Referred to Data Sheet

Cc-Vbc(PNP)

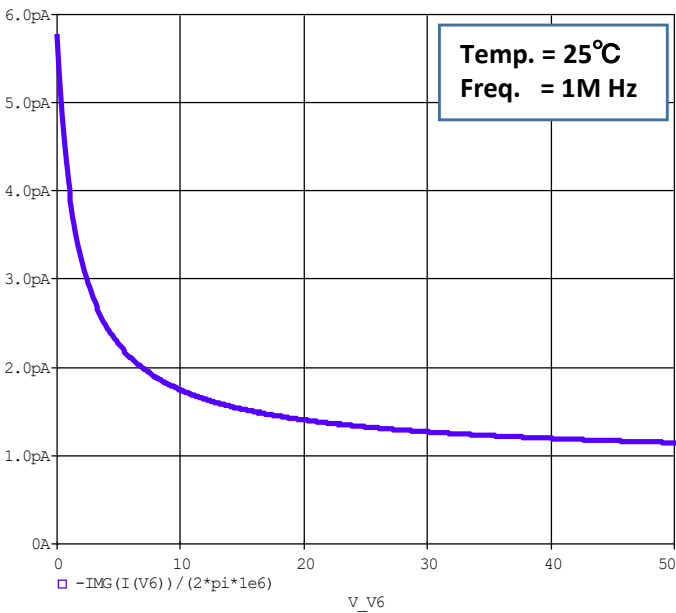


fT-IC(PNP)

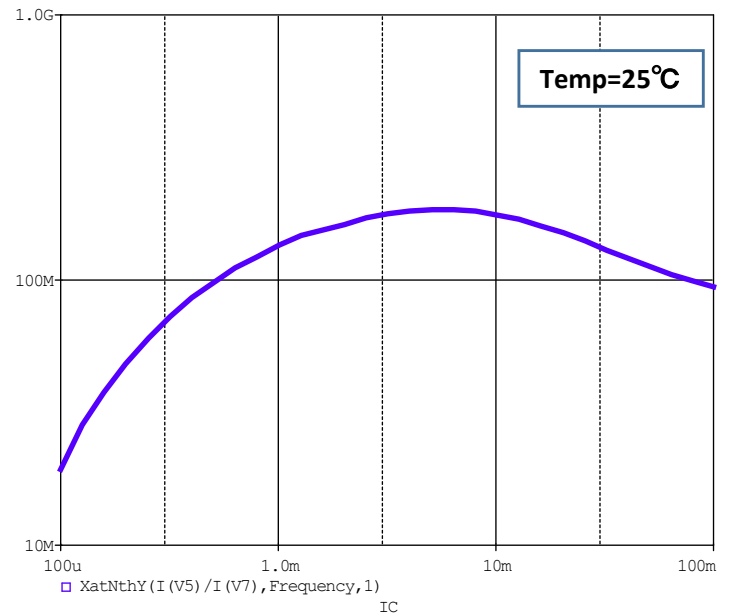


Simulation results are following.  
Explanatory notes — : simulated

Cc-Vbc(PNP)



fT-IC(PNP)



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